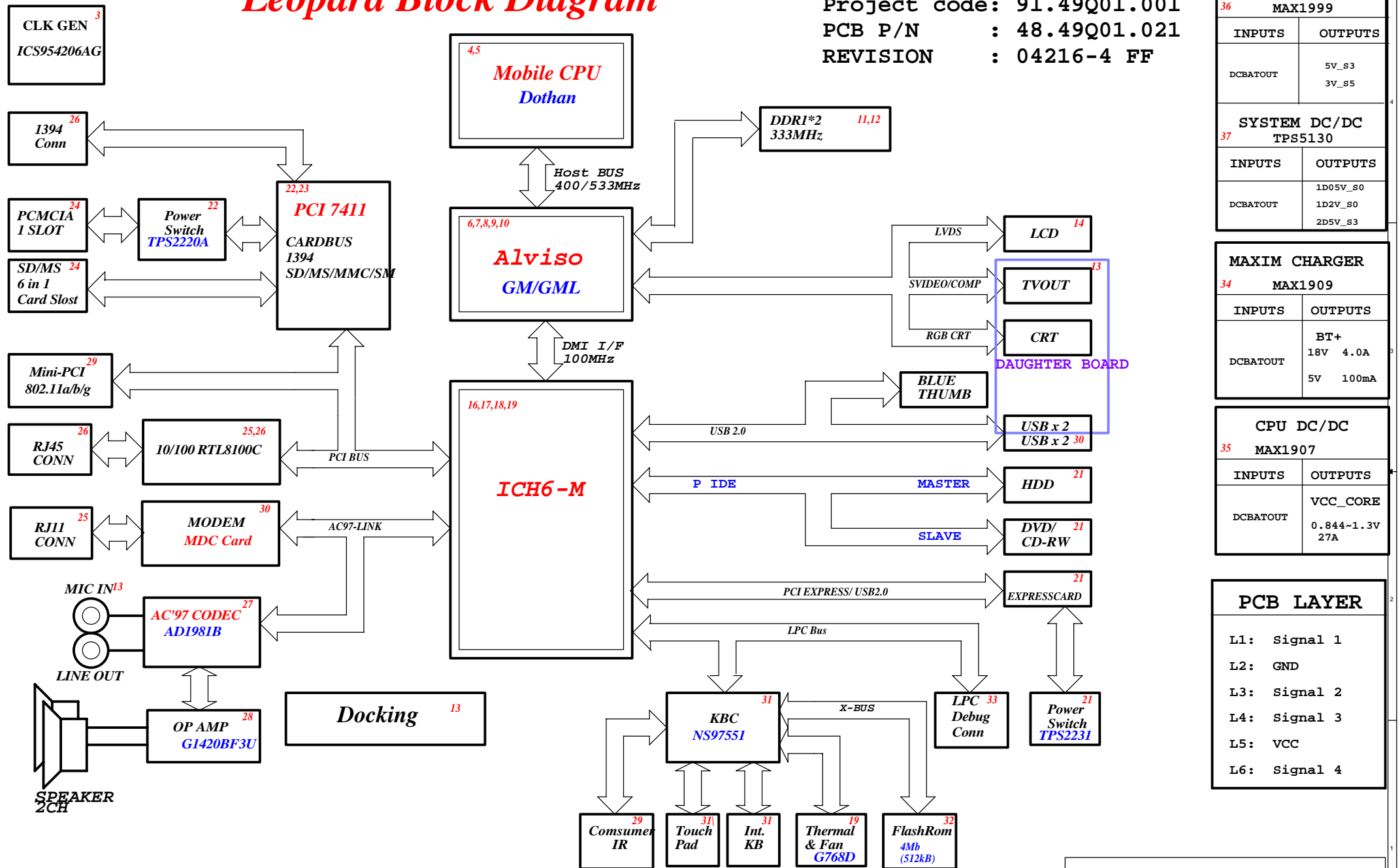


Leopard Block Diagram

Project code: 91.49Q01.001
PCB P/N : 48.49Q01.021
REVISION : 04216-4 FF



ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

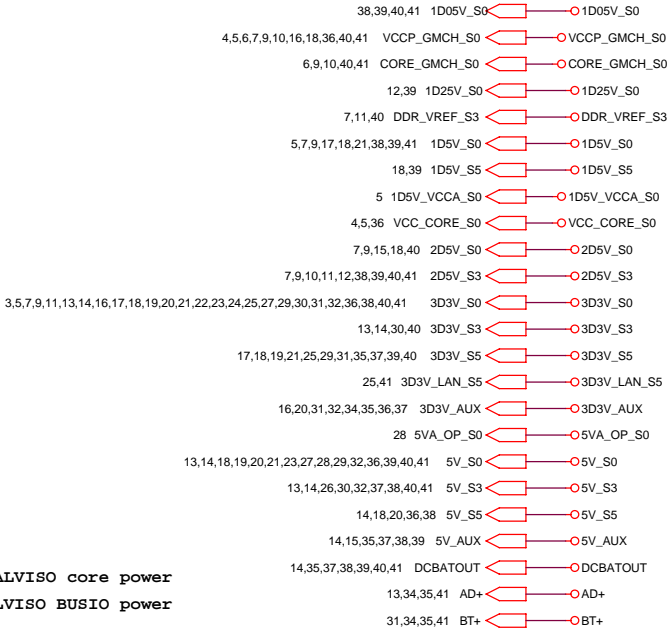
ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

Power name description

5V_S0= 5 Voltage power up on system work(S0 state)
5V_S3= 5 Voltage suspend to RAM(S3 state)
5V_S5= 5 Voltage soft off(S5 state)
3D3V_S0= 3.3 Voltage power up on system work(S0 state)
3D3V_S3= 3.3 Voltage suspend to RAM(S3 state)
3D3V_S5= 3.3 Voltage soft off(S5 state)
LVDDR_2D5V= 2.5 Voltage power up on system work(S0 state)
2D5V_S3= 2.5 Voltage suspend to RAM(S3 state)
2D5V_S0= 2.5 Voltage power up on system work(S0 state)

VCC_CORE_S0= CPU VID Voltage power up on system work(S0 state)
1D5V_VCCA_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S5= 1.5 Voltage soft off(S5 state)
DDR_VREF_S3= 1.25 Voltage suspend to RAM(S3 state)
1D25V_S0= 1.25 Voltage power up on system work(S0 state)
1D2_VGA_S0= 1.2 Voltage power up on system work(S0 state) for VGA
1D05V_S0= 1.05 Voltage power up on system work(S0 state)
CORE_GMCH_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power
VCCP_GMCH_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power



PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD21	P_INTE#	REQ0# / GNT0#
Cardbus Controller TI7411	AD22	(CARBUS)P_INTG# (1394)P_INTF# (CARD READER)P_INTG#	REQ1# / GNT1#
LAN	AD23	P_INTE#	REQ2# / GNT2#
Blue Thumb	AD24		

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

ITP

Size

Document Number

Rev

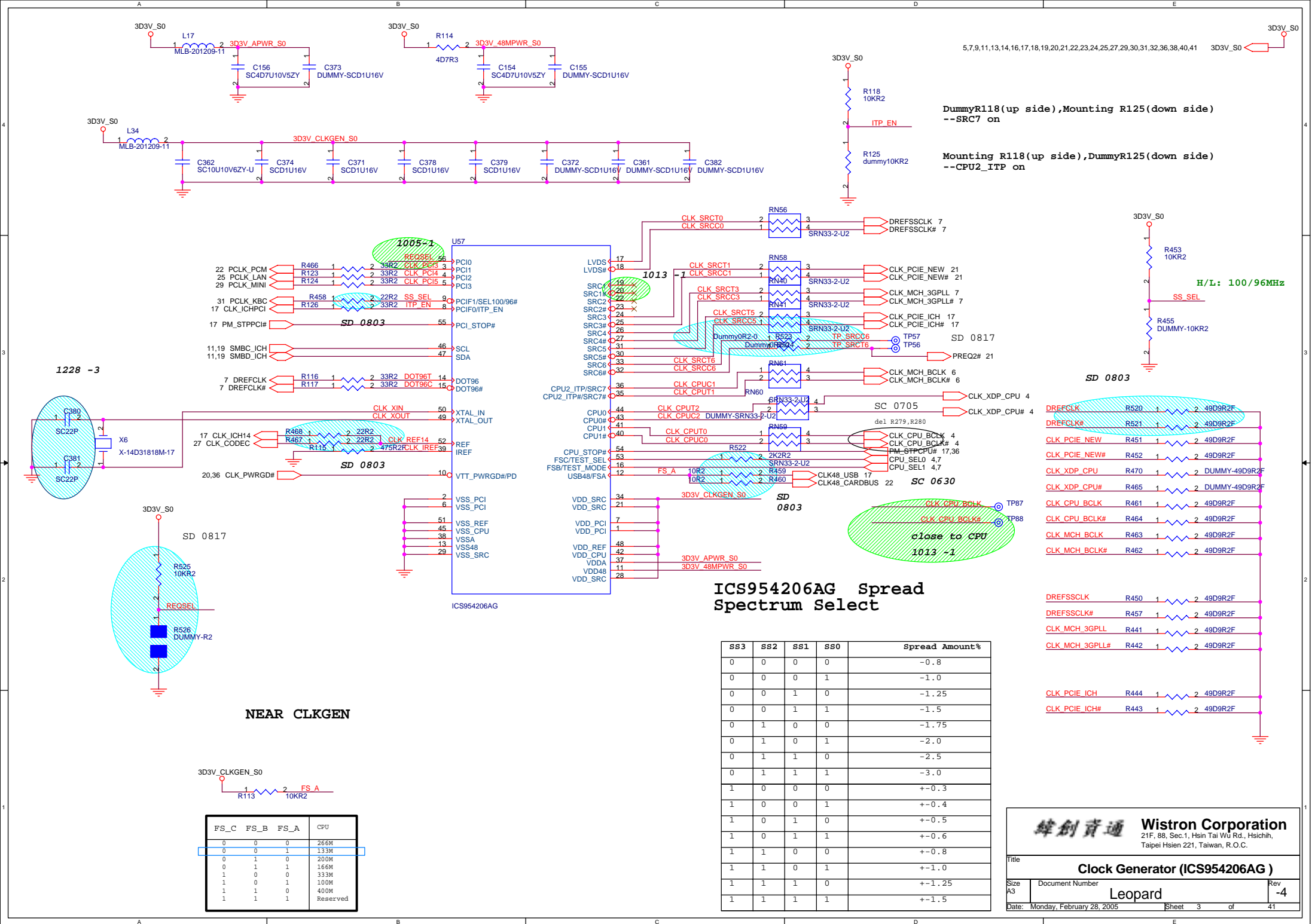
A3

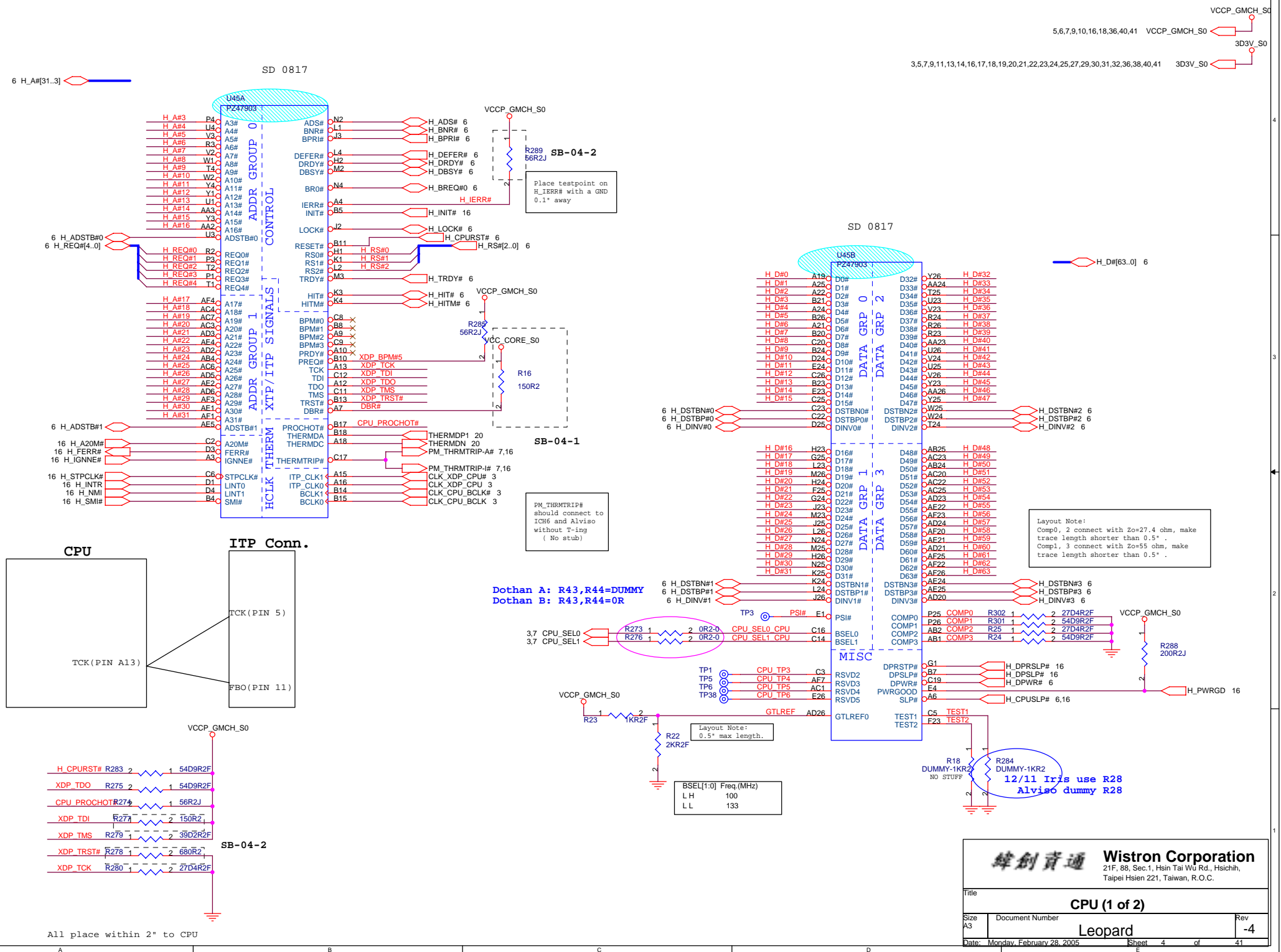
Leopard

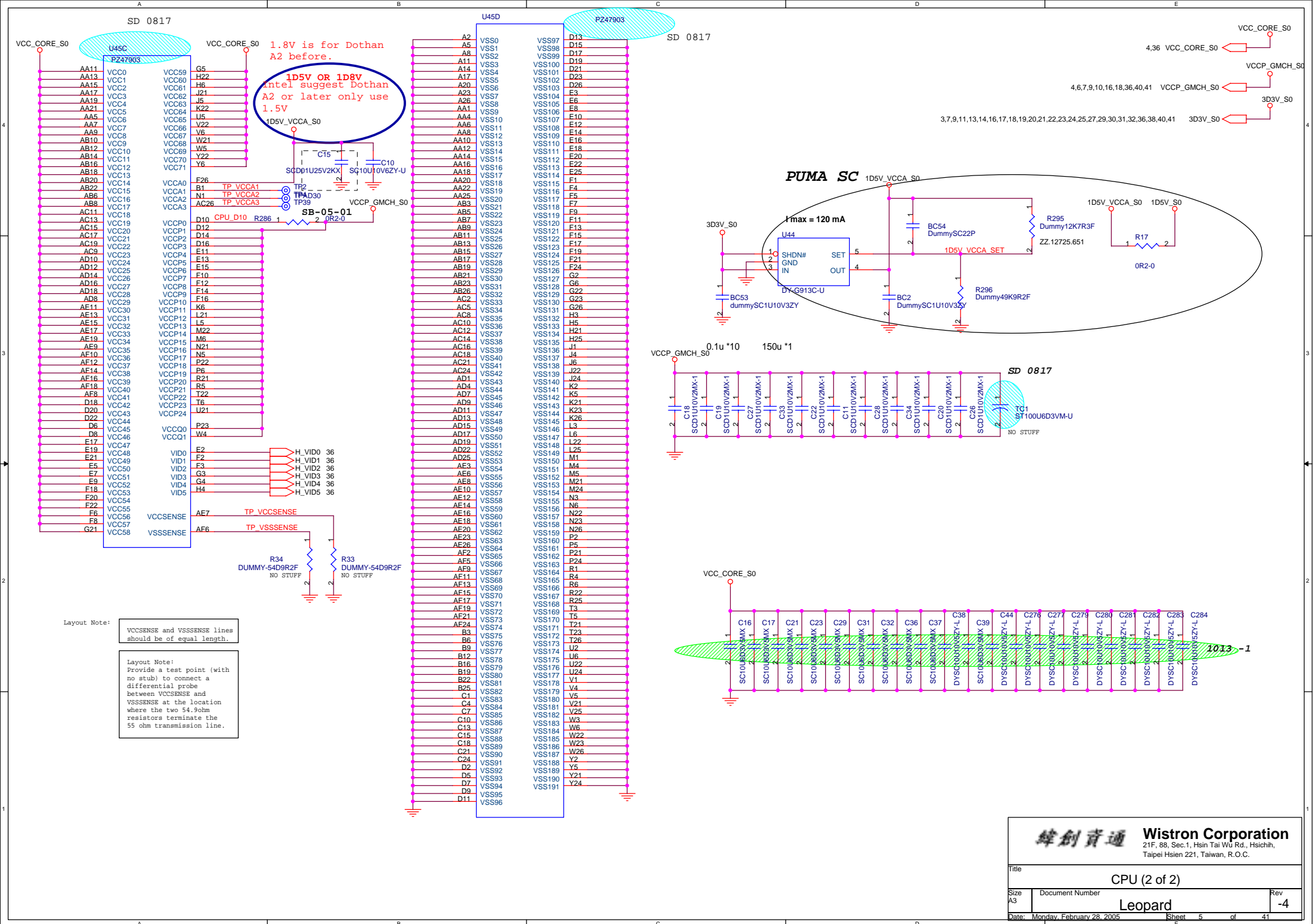
-4

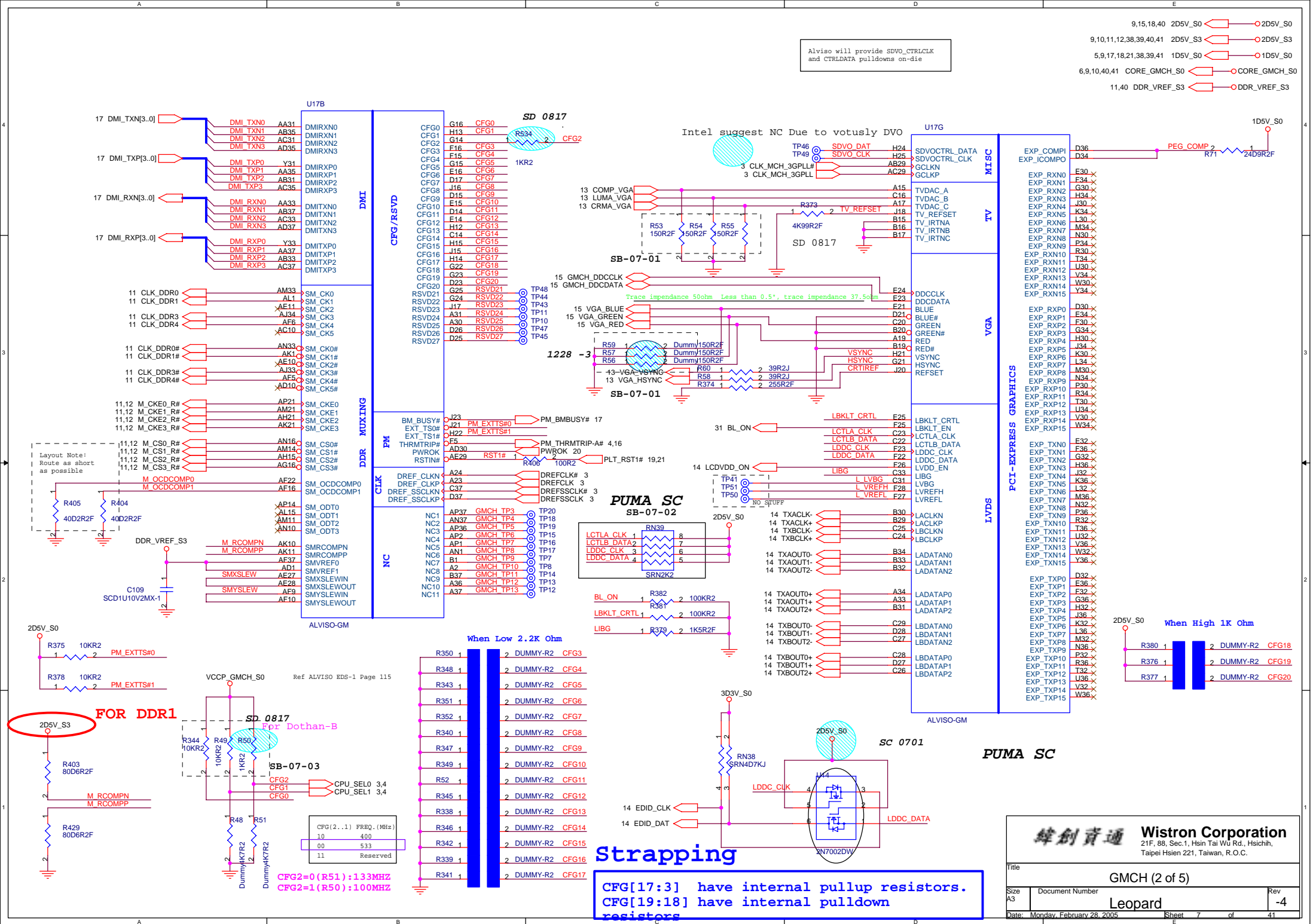
Date: Sunday, February 27, 2005

Sheet 2 of 41

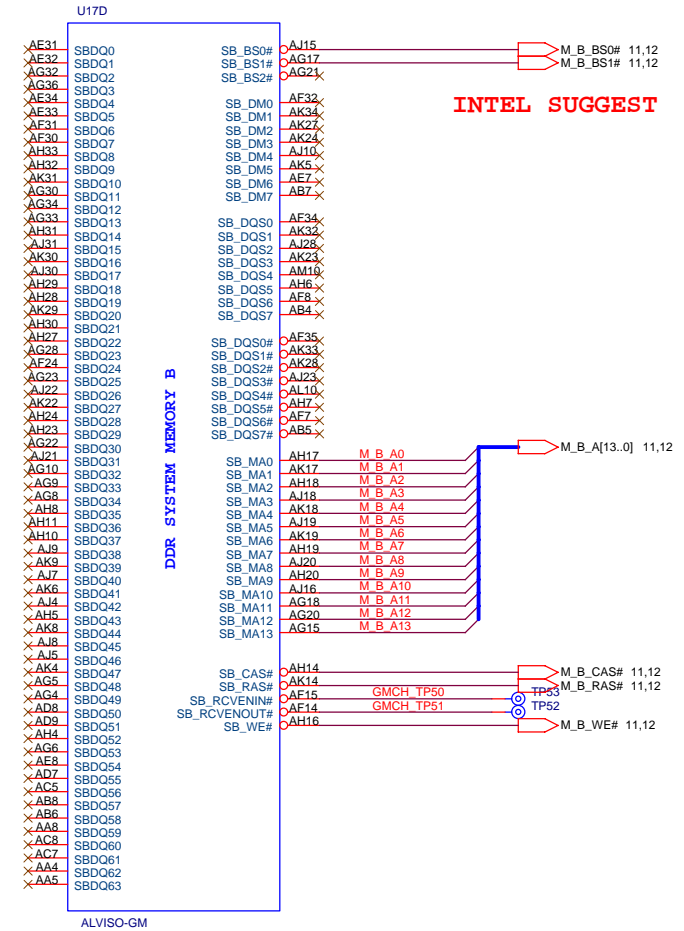
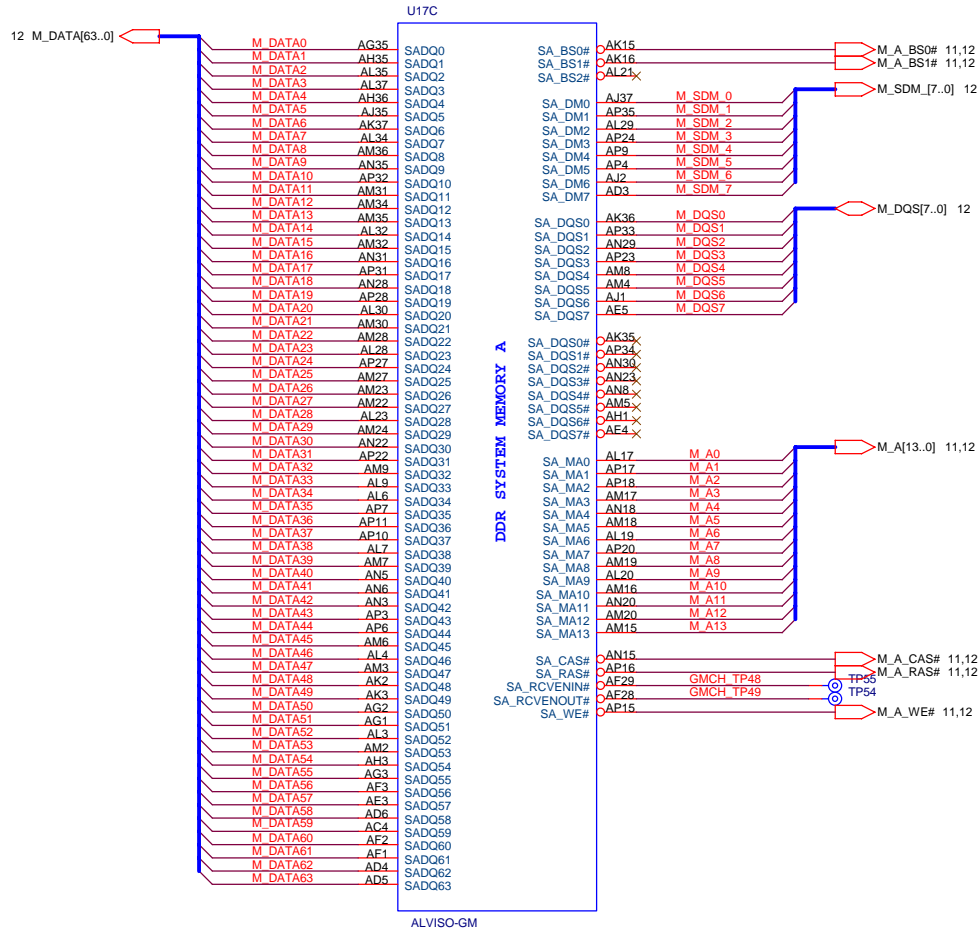




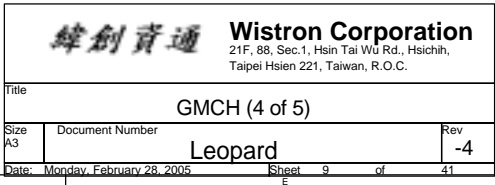


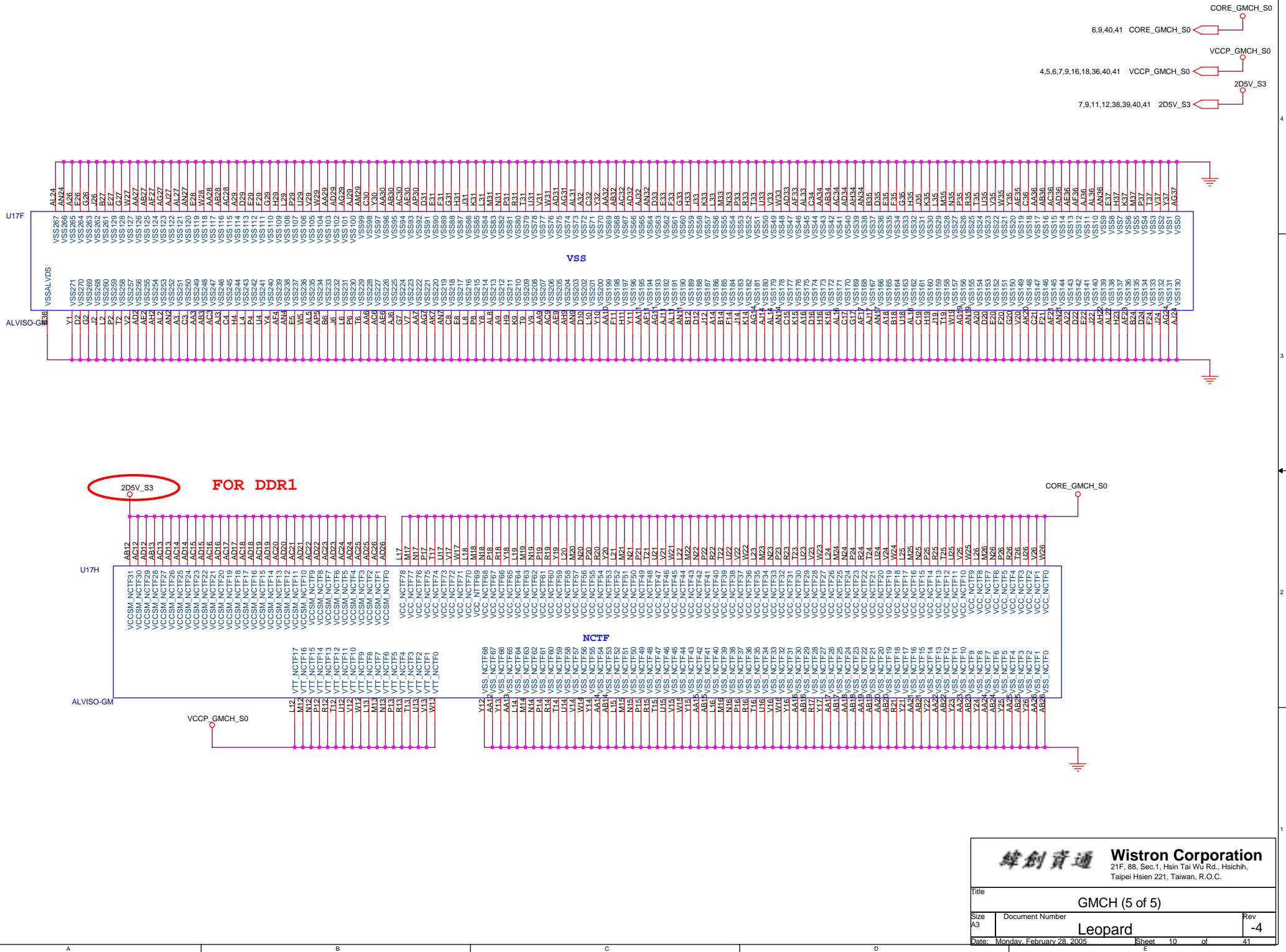


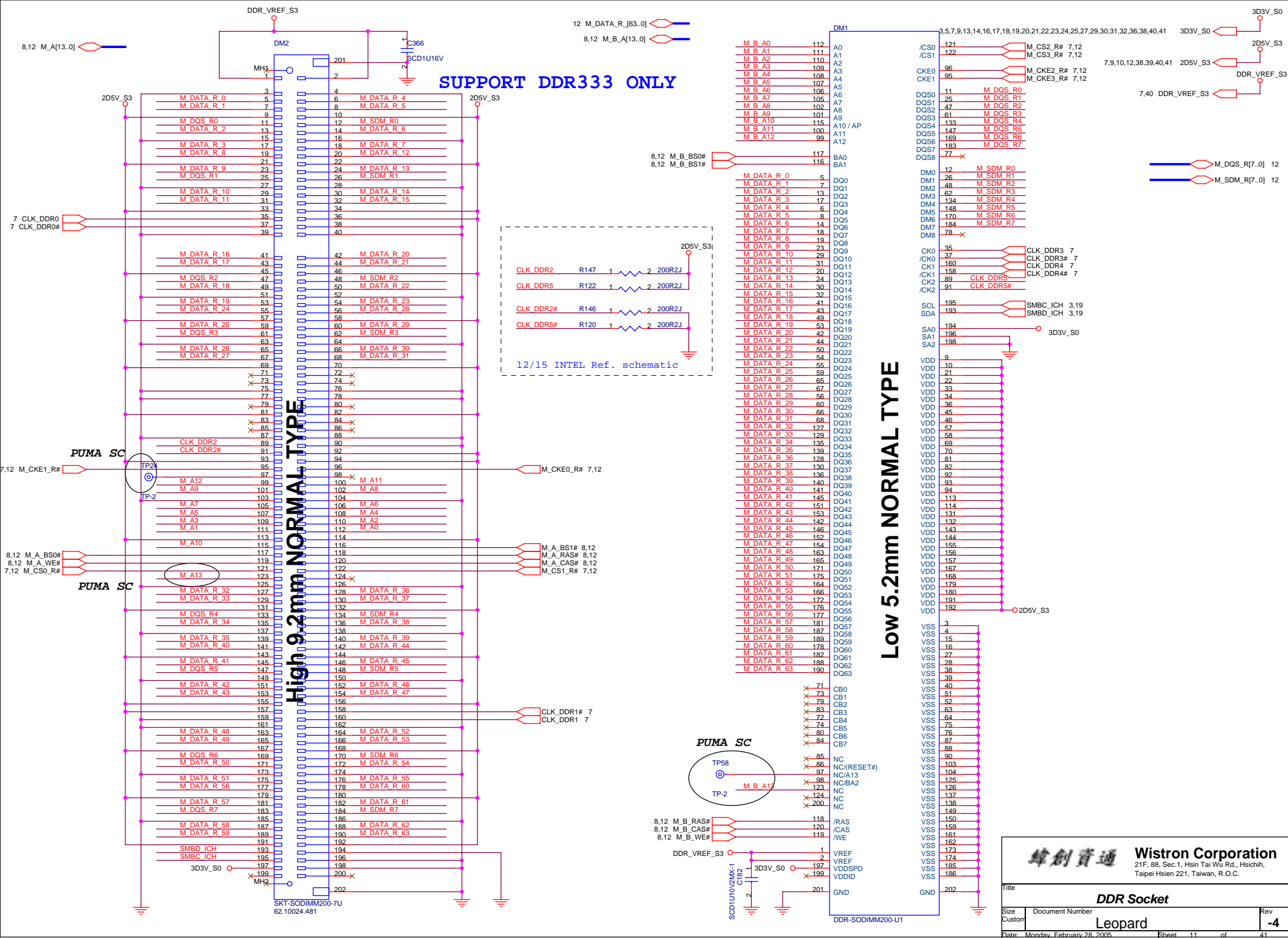
SUPPORT DDR333 ONLY



INTEL SUGGEST



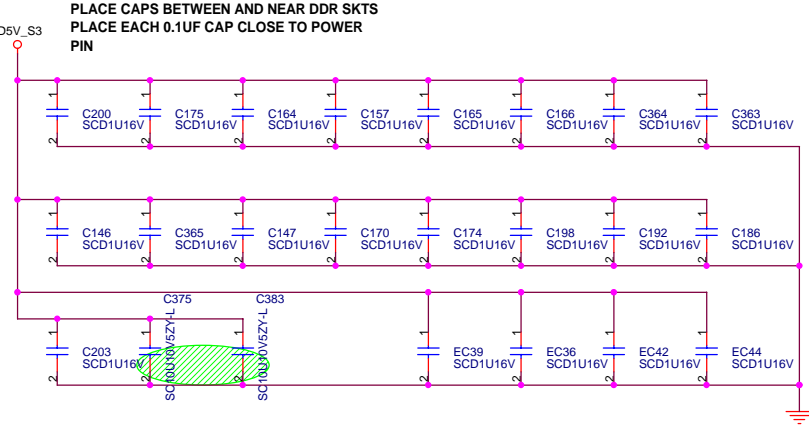
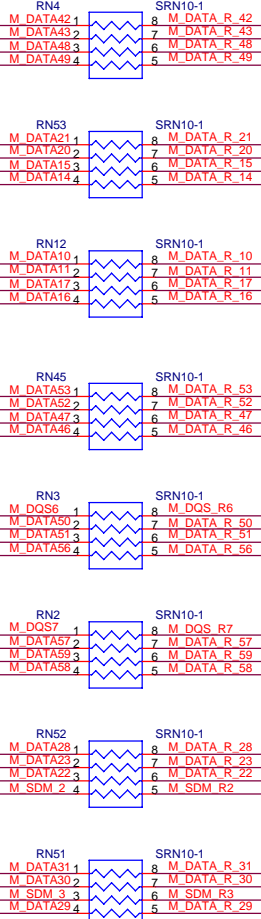
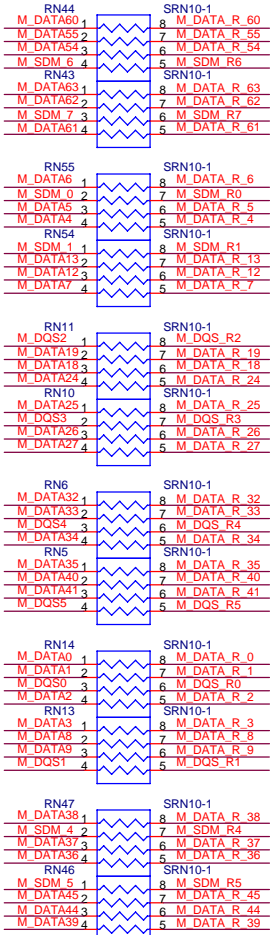




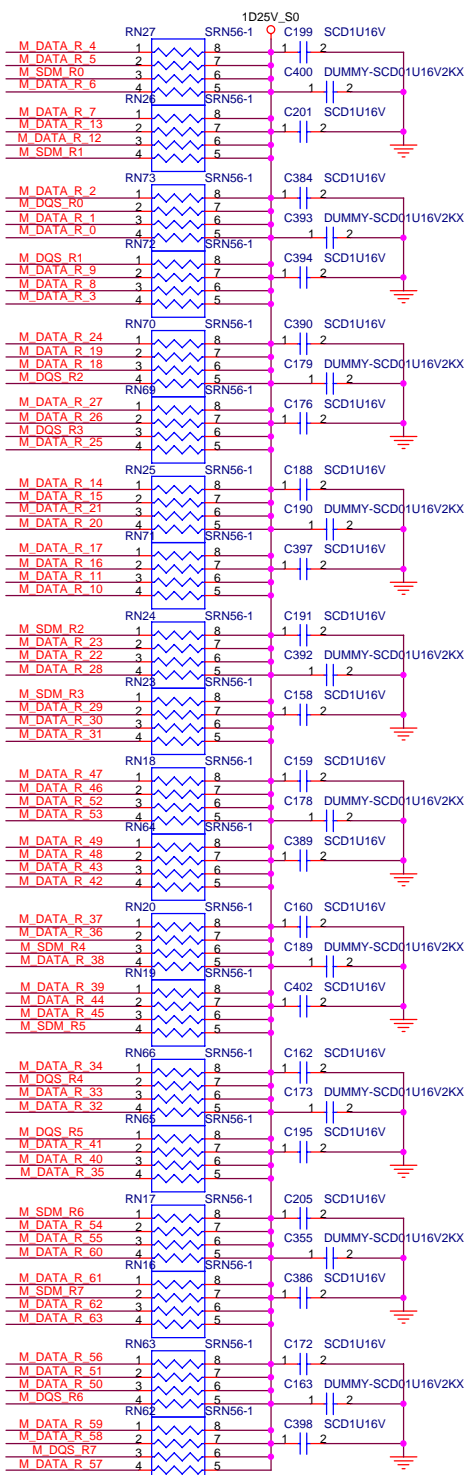
SERIES DAMPING

PUMA-SC

Change RN to small size

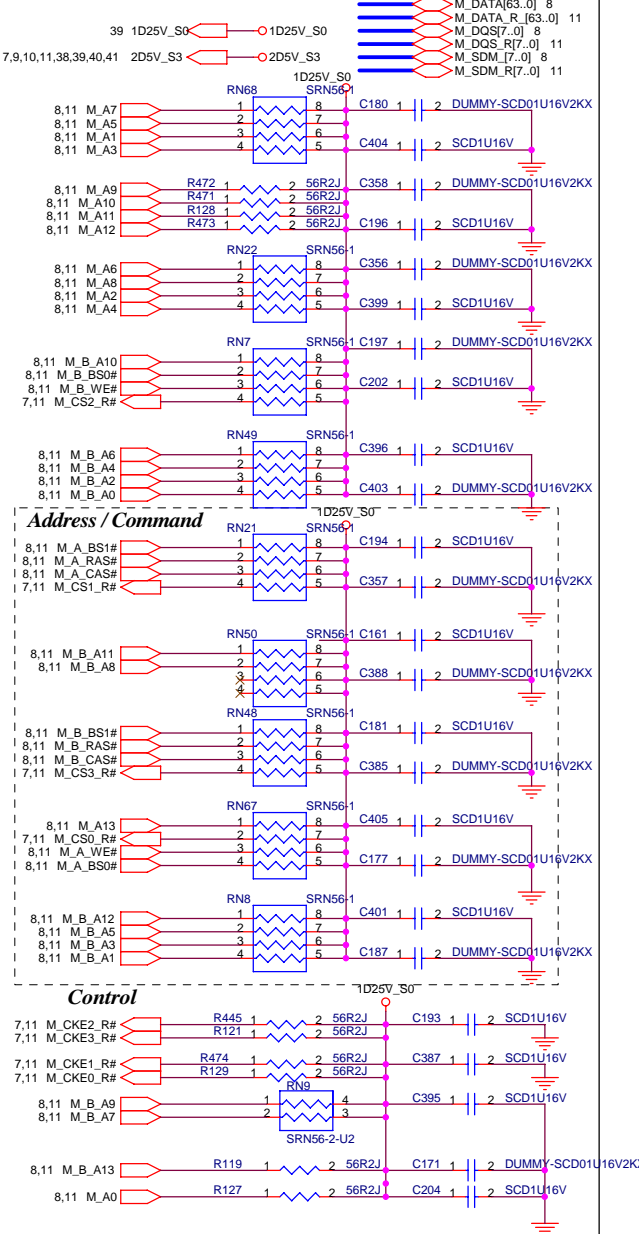


PLACE CAPS BETWEEN AND NEAR DDR SKTS
PLACE EACH 0.1UF CAP CLOSE TO POWER
PIN



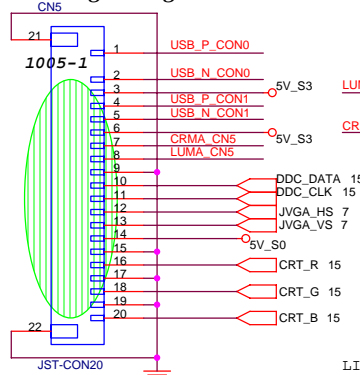
PARALLEL TERMINATION

PULL HIGH STUBS <0.8", PLACE RPs CLOSE TO DM2
NO EQUAL LENGTH LIMITATION

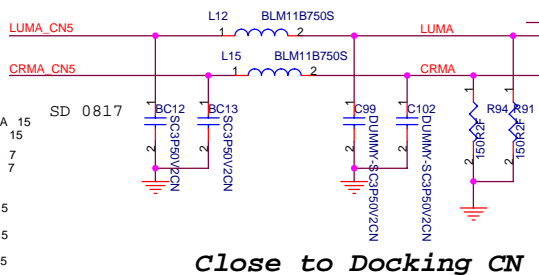


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

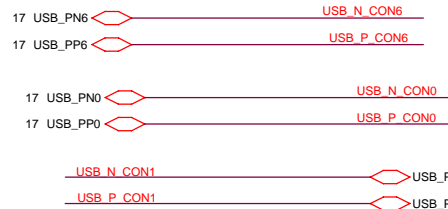
Digital Signal CONN



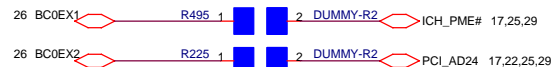
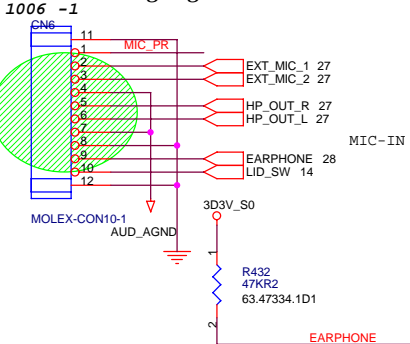
PUMA SC



Close to Docking CN

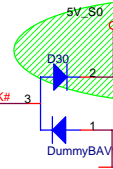
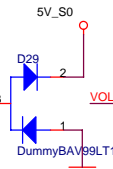
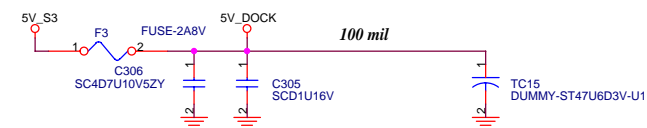
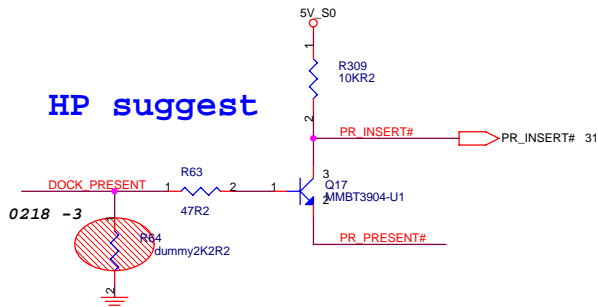


Analog Signal CONN

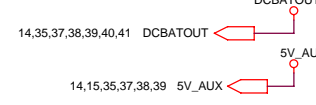
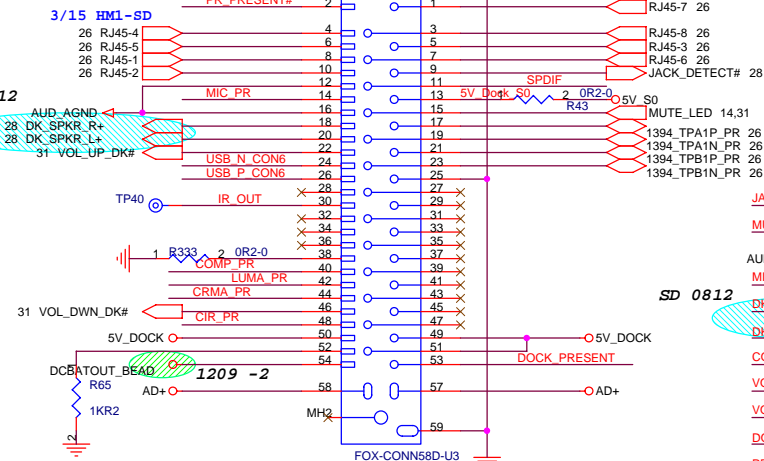
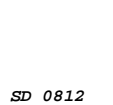


Please close to ICH6

HP suggest

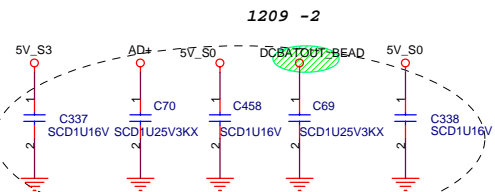
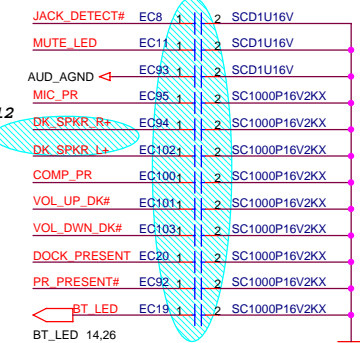


Docking Connector

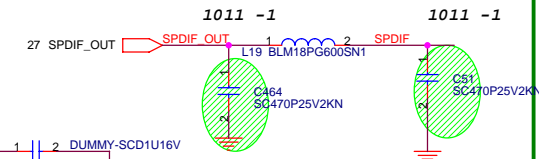


SD 0812

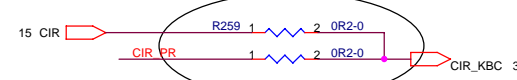
HMI-SD FOR EMI



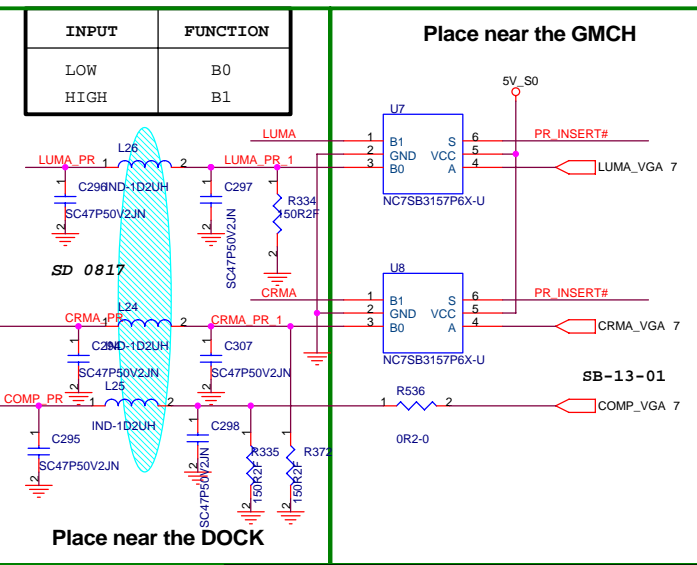
PUMA SC



PUMA SC



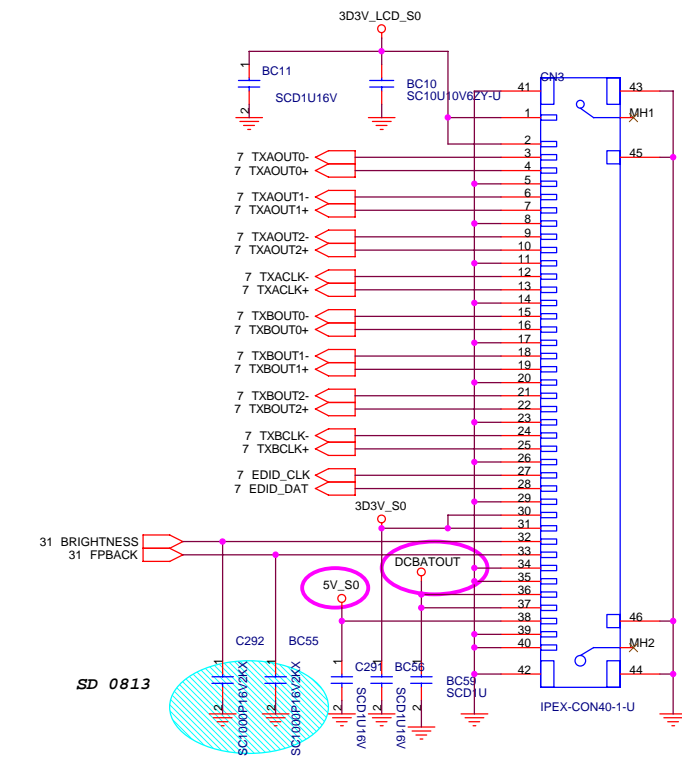
CIR,CIR_PR,CIR_KBC are connect together. default setting 12/12



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipai Hsien 221, Taiwan, R.O.C.

Title		Board to board conn/ Docking	
Size	A3	Document Number	Leopard
Date:	Monday, February 28, 2005	Sheet	13 of 41

INVERTER/LCD

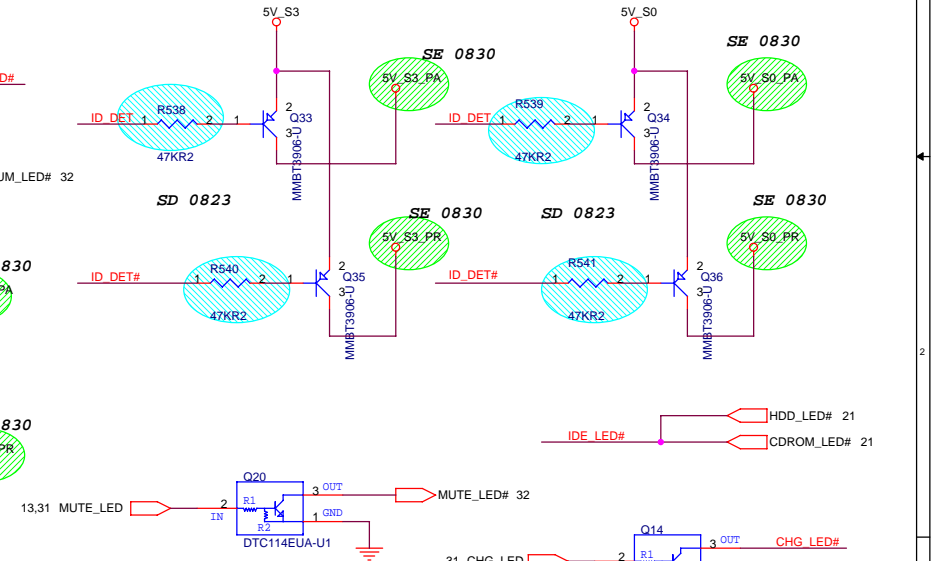
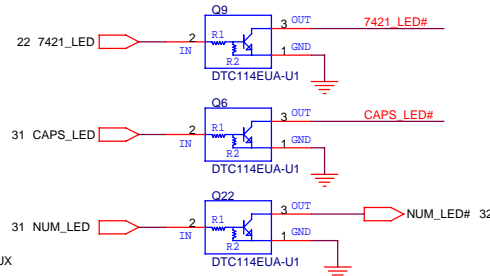
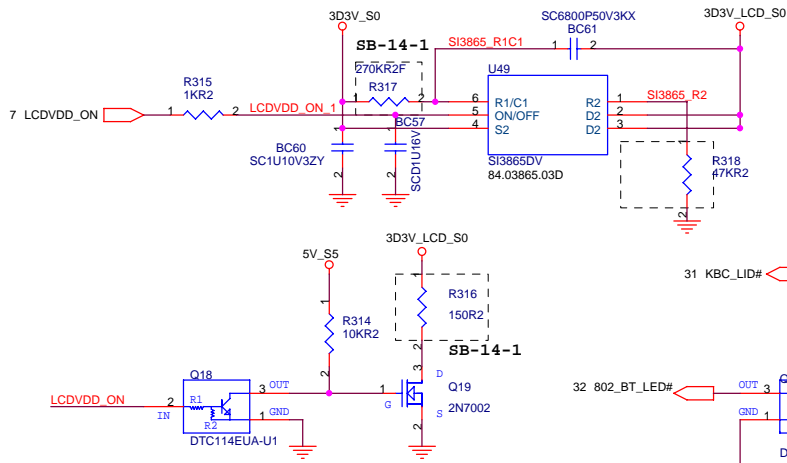
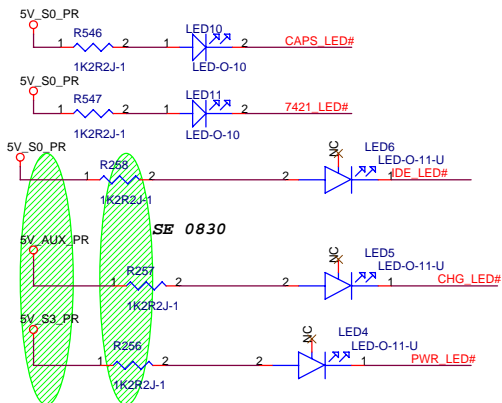


	PWR	CHR	HDD	IR	CAPS	7421
PR Botton	Amber LED4	Amber LED5	Amber LED6	U42	Amber LED1	Amber LED2
PA Top	Blue LED8	Blue LED7	Blue LED9	U64	Blue LED1	Blue LED2

SC 0705

change R from 100 to 200 ohm

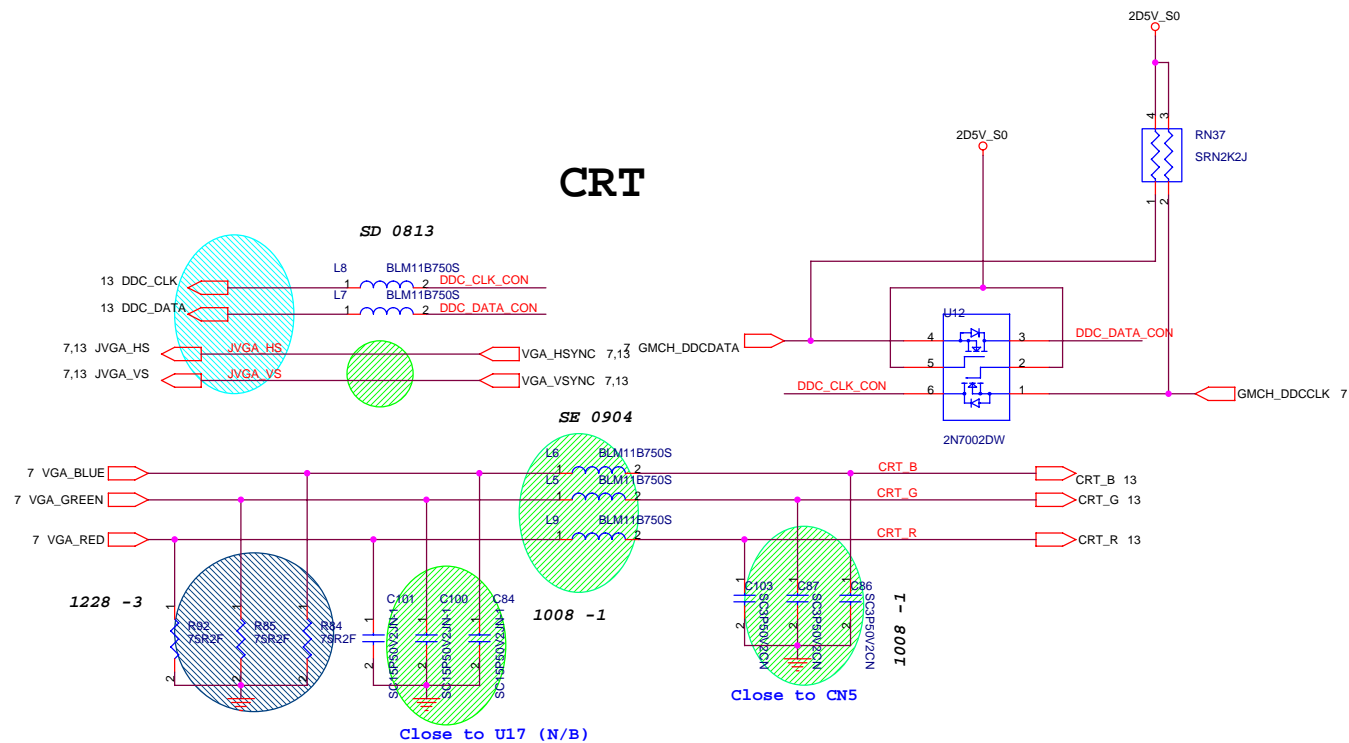
PUMA SC



PA & PR diffent parts

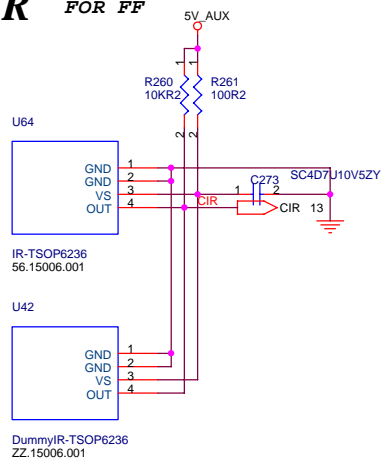
	PA	PR
LED1	83.00190.Y70	83.00190.W70
LED2	83.00190.Y70	83.00190.W70
LED4	Dummy	83.00110.D70
LED5	Dummy	83.00110.D70
LED6	Dummy	83.00110.D70
LED7	83.00110.E70	Dummy
LED8	83.00110.E70	Dummy
LED9	83.00110.E70	Dummy
U64	56.15006.001	Dummy
U42	Dummy	56.15006.001
R256	63.20134.1D1	63.12234.1D1
R257	63.20134.1D1	63.12234.1D1
R258	63.20134.1D1	63.12234.1D1
R93	63.20134.1D1	63.12234.1D1
R112	63.20134.1D1	63.12234.1D1

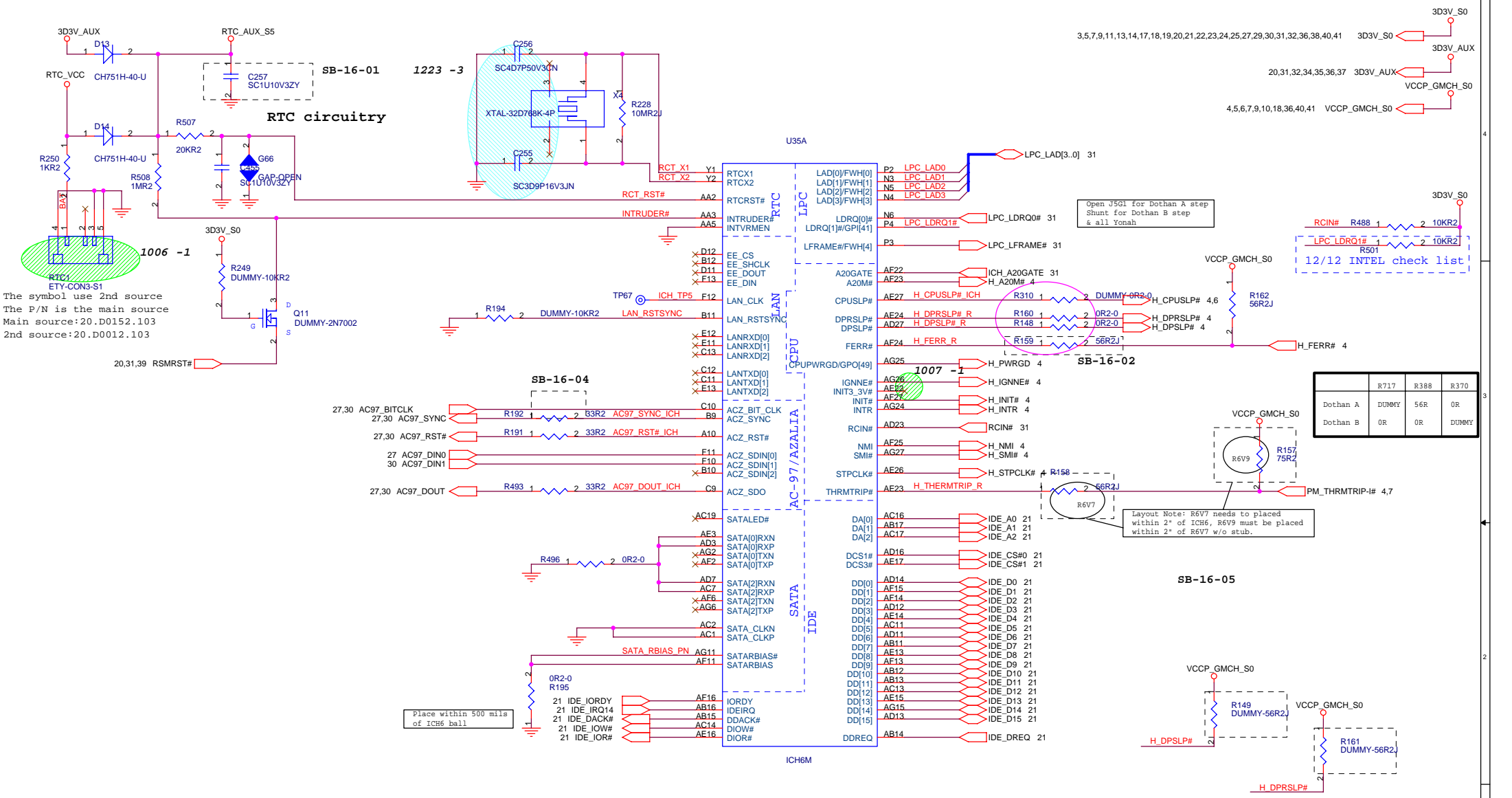
CBUS1	21.H0088.001	21.H0088.001
R176	63.10334.1D1	Dummy
R177	Dummy	63.10334.1D1

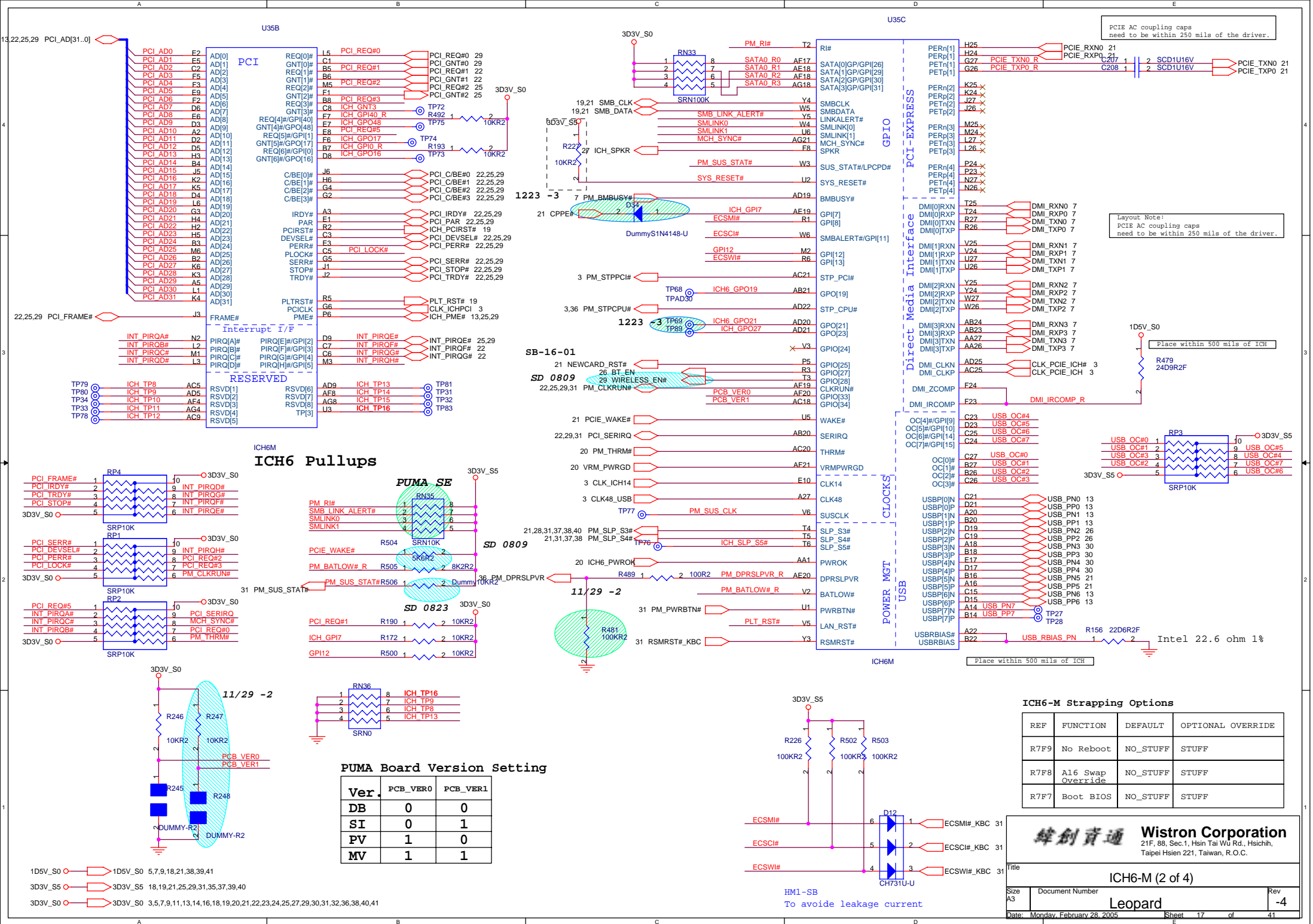


010804 Modified on Astro ID request

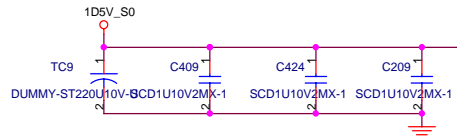
CIR FOR FF



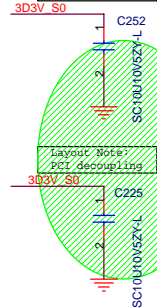




Layout Note:
Place above caps within
100 mils of ICH near F27, P27, AB27

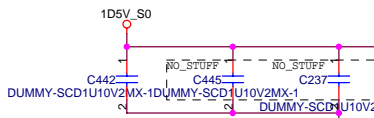


Layout Note:
IDB decoupling



1013 -1

Place within 100
mils of ICH
near pin AG5



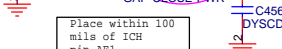
Place within 100
mils of ICH
near pin AG9



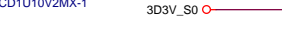
Place within 100
mils of ICH



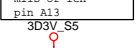
Place within 100
mils of ICH
near E26, E27



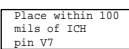
Place within 100
mils of ICH
pin AG10



Intel dummy



Place within 100
mils of ICH
pin A13



U35E

CORE

IDE

PCI

USB

USB CORE

PCI/IDE

REF

ICH6M

ICH6M

ICH6M

ICH6M

ICH6M

ICH6M

ICH6M

ICH6M

ICH6M

ICH6M

ICH6M

ICH6M

ICH6M

ICH6M

ICH6M

ICH6M

ICH6M

ICH6M

ICH6M

ICH6M

ICH6M

ICH6M

ICH6M

ICH6M

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_B

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC1_5_A

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

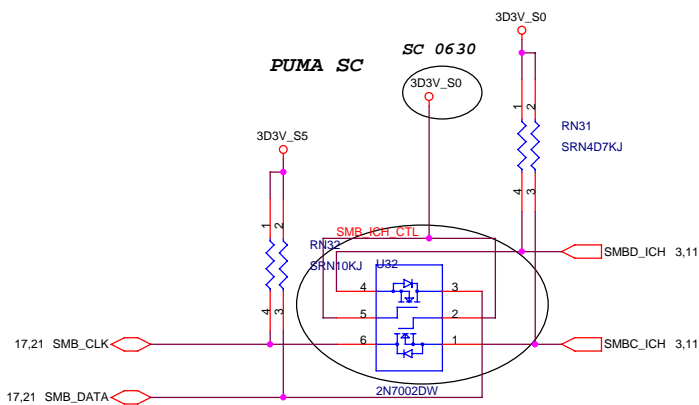
VCC3_3

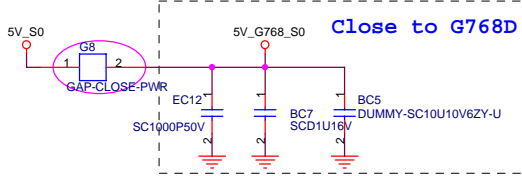
VCC3_3

VCC3_3

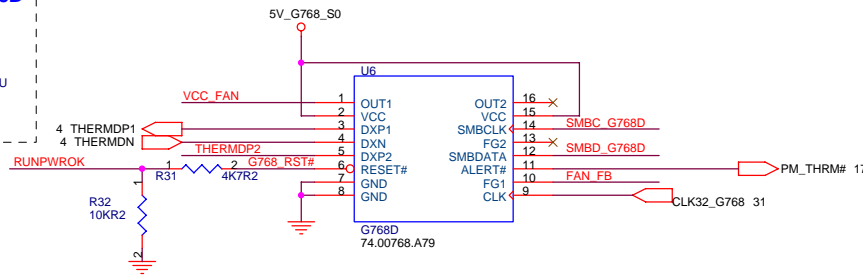
VCC3_3

VCC3_3

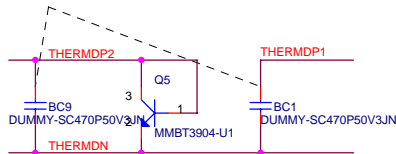




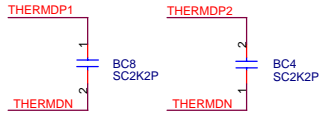
Reserve for G768B
works at High
Speed



Put these two Caps near the thermal diode.

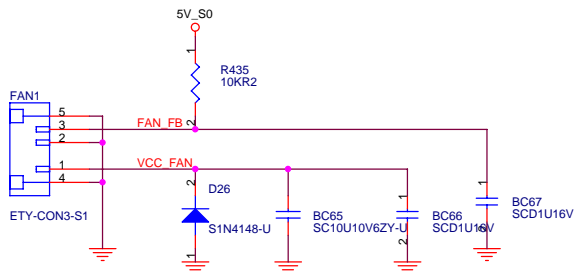


SYSTEM SENSOR



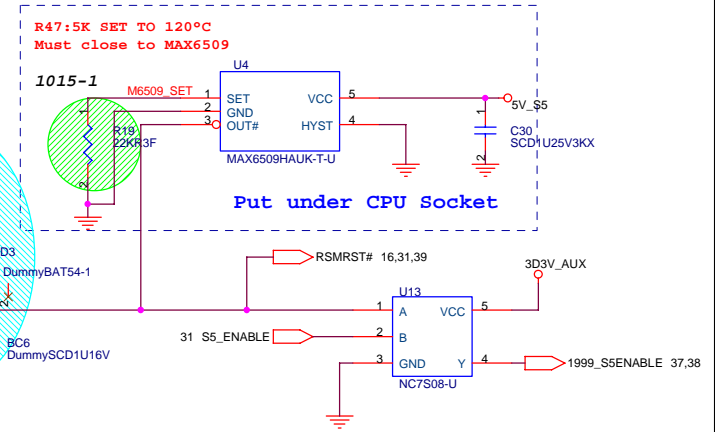
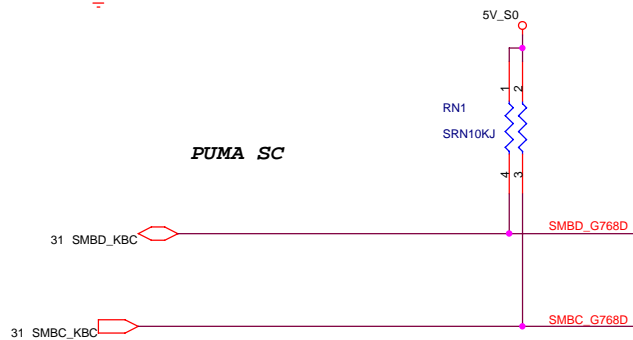
THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768B

180 ms after VCC_G768 > 4.38v, p2, 7



The symbol use 2nd source
The P/N is the main source
Main source:20.D0152.103
2nd source:20.D0012.103

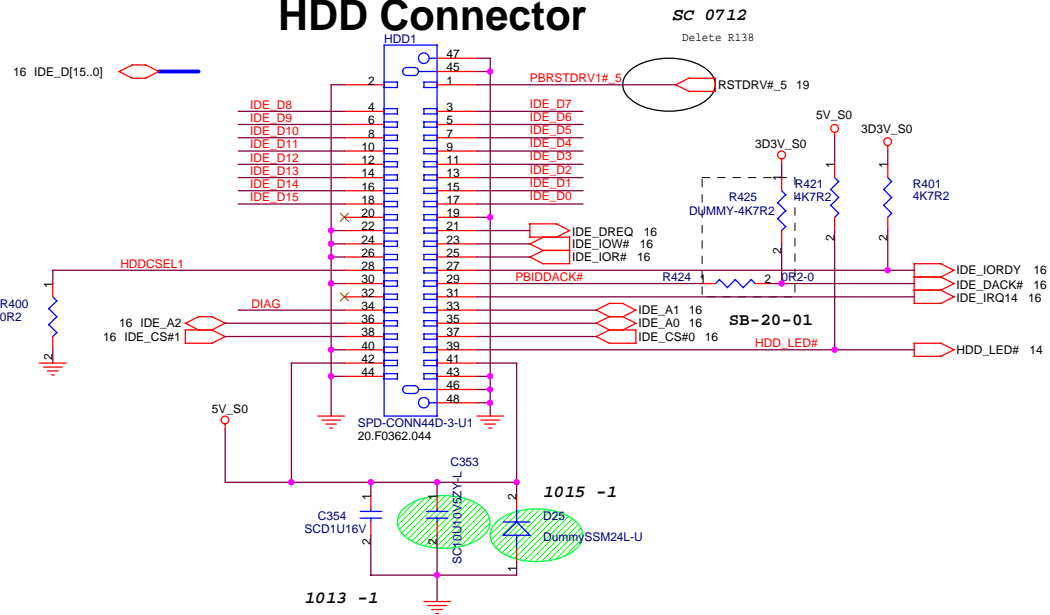
PUMA SC



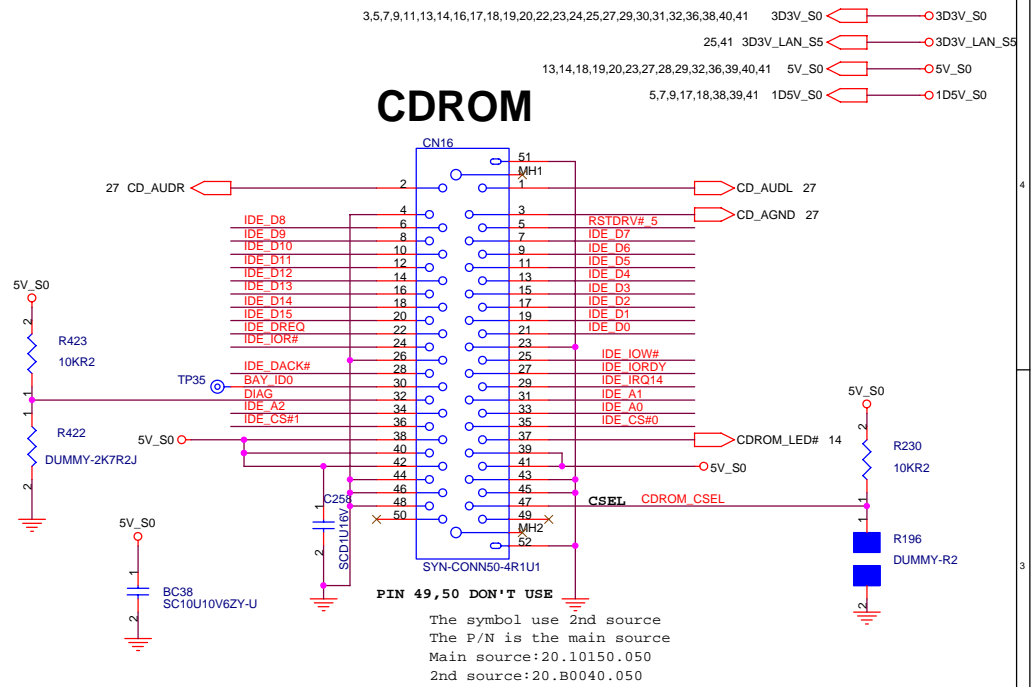
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

Title			G768D	
Size	Document Number	Leopard		Rev
A3				-4
Date:	Monday, February 28, 2005	Sheet	20	of 41

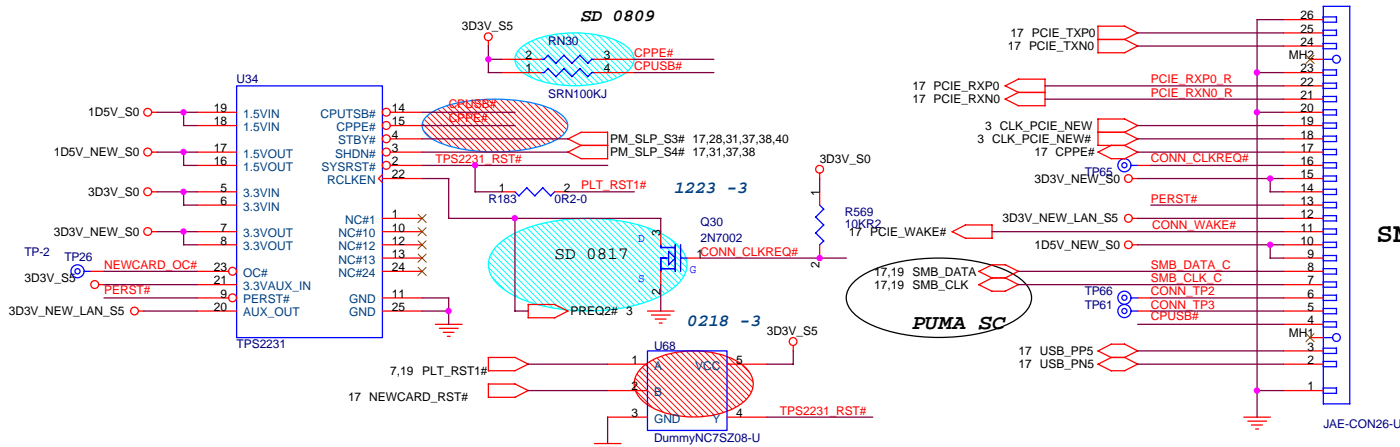
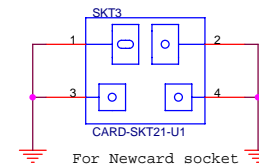
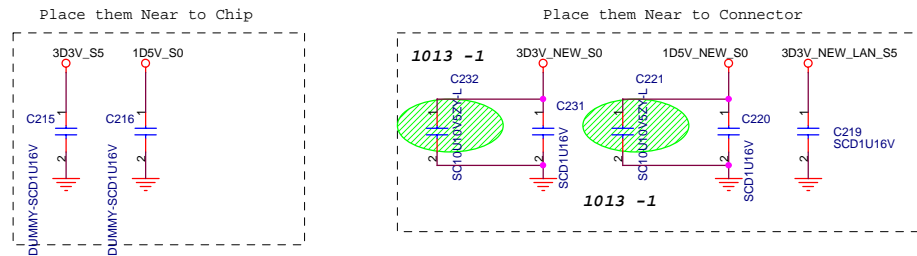
HDD Connector



CDROM

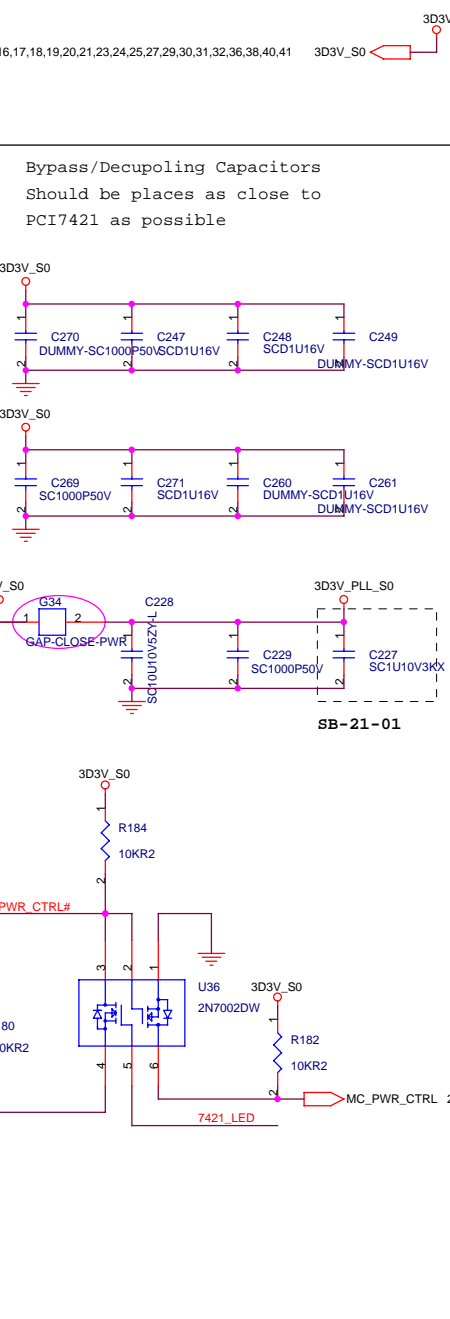
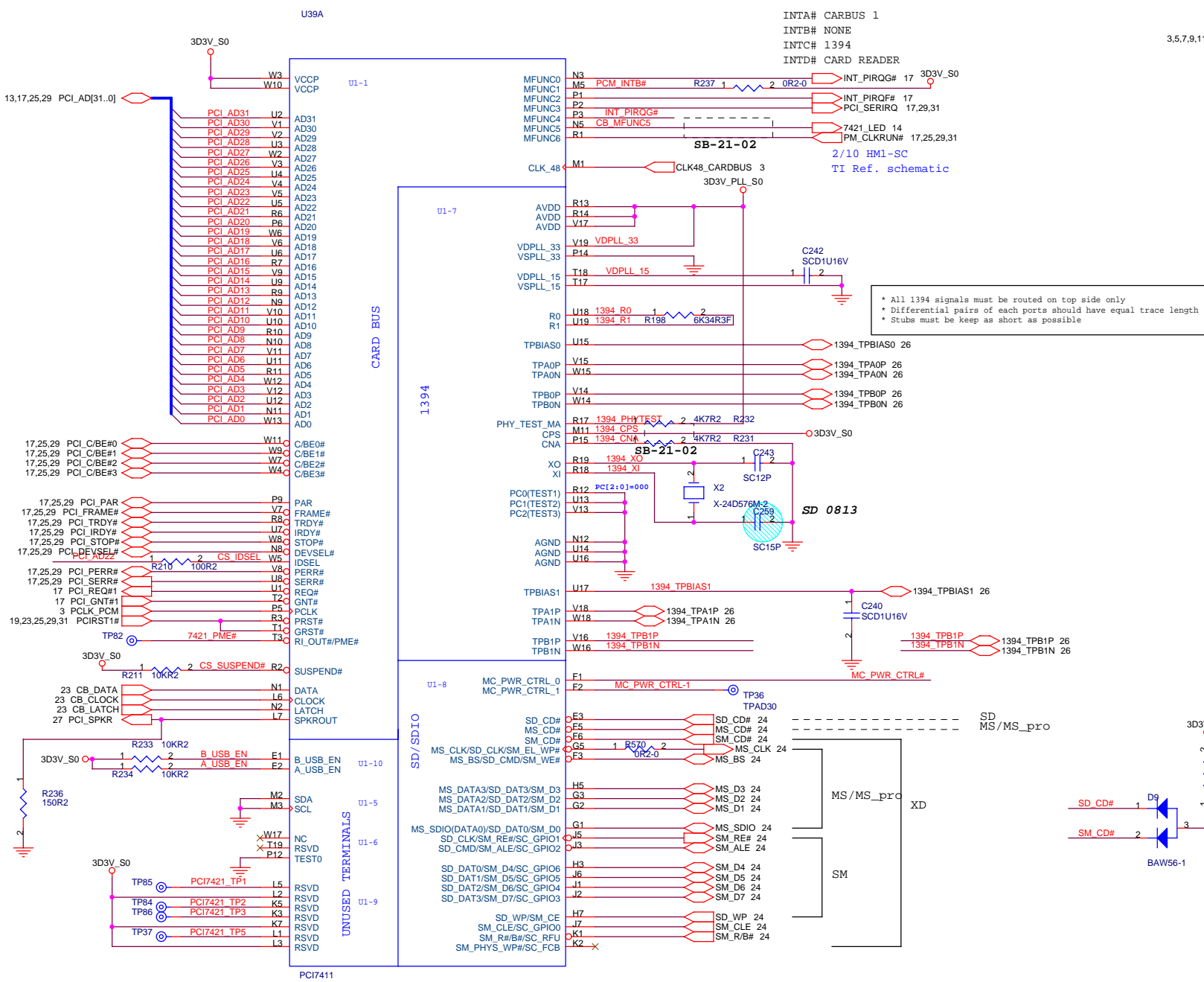


NEWCARD Connector



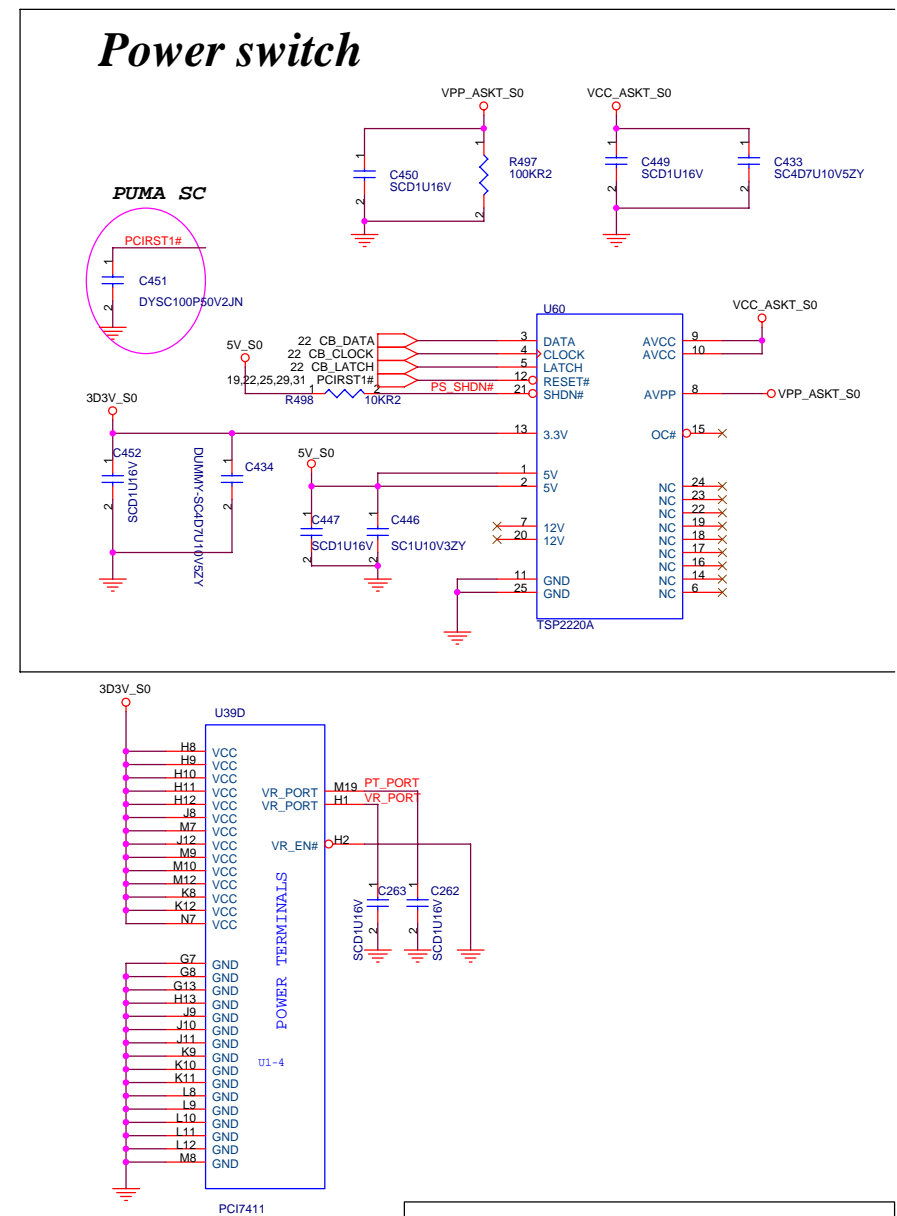
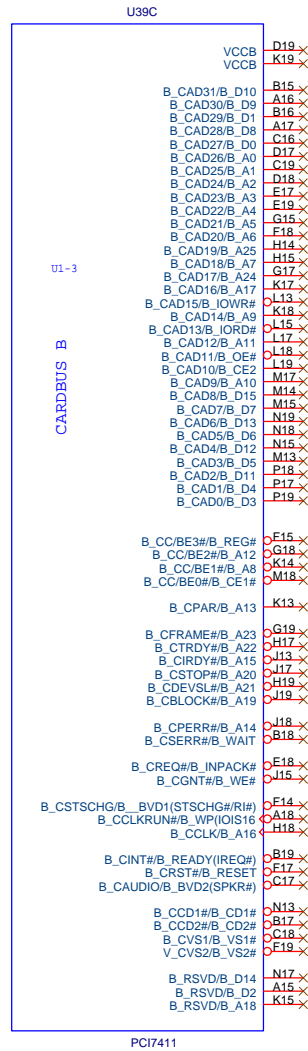
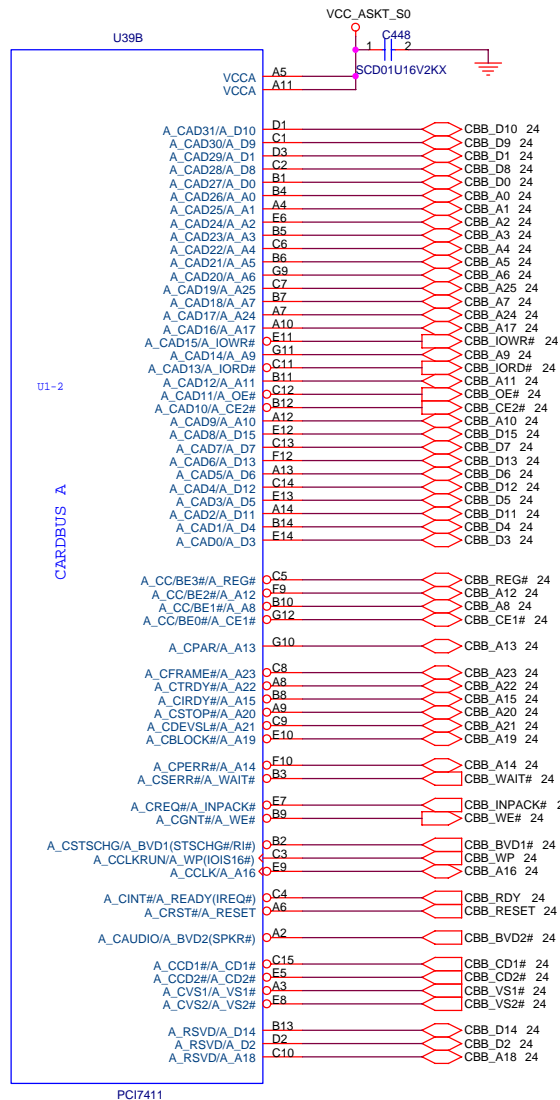
SMBUS (ICH6--NEWCARD, LAN)



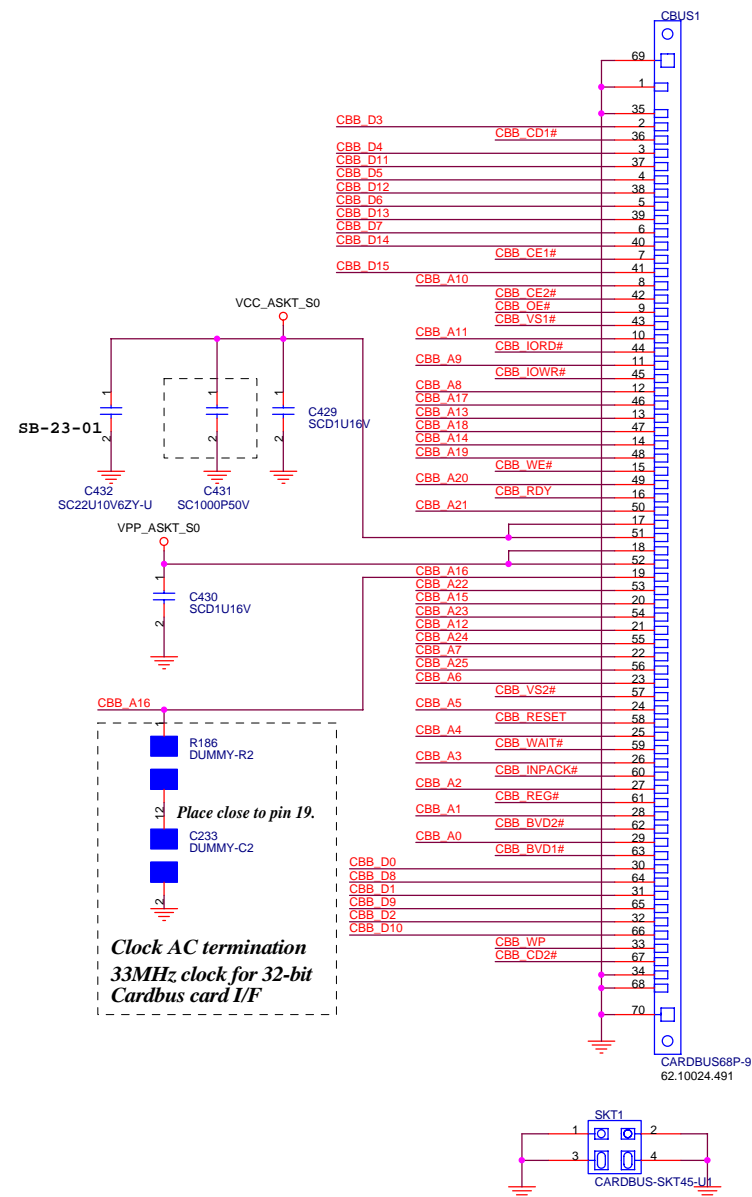


7411:71.07411.00U
7421:71.07421.00U

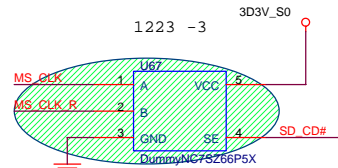
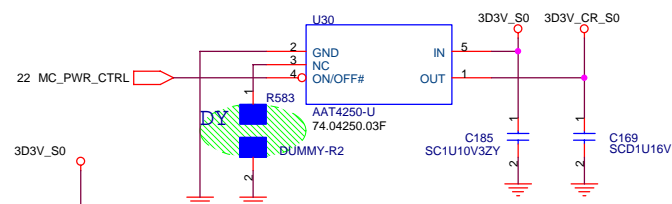
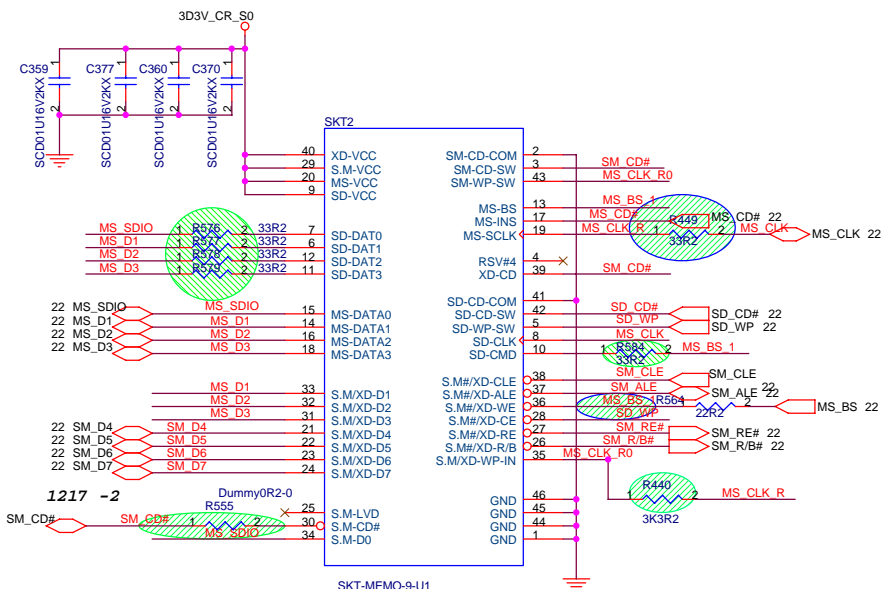
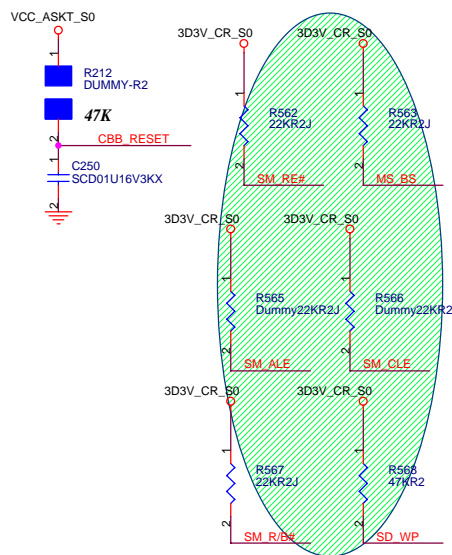
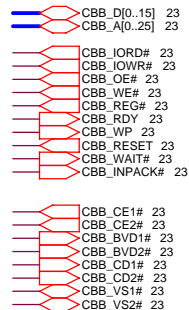
HM1-SE
TI
update
sepc.



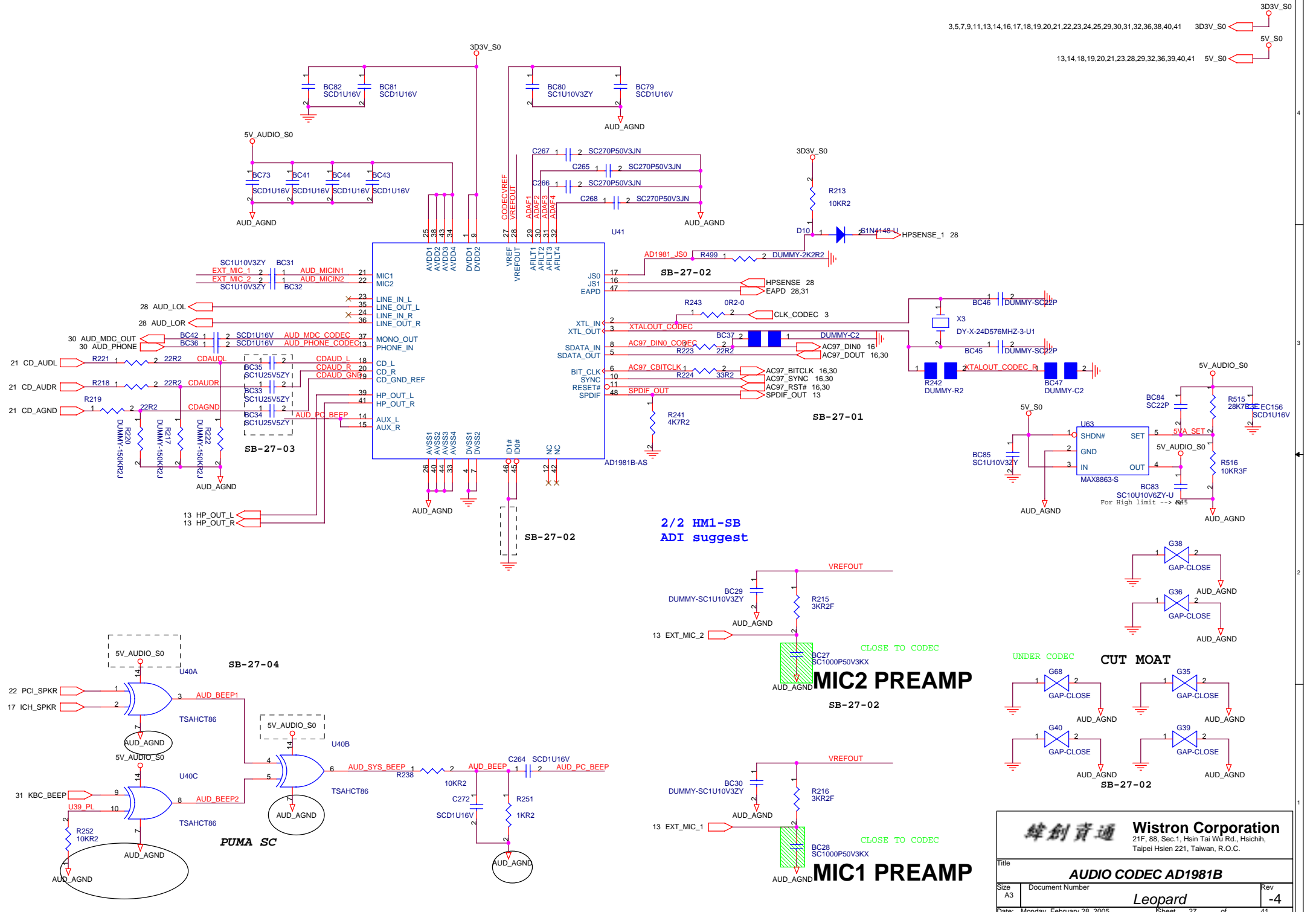
PCMCIA Socket



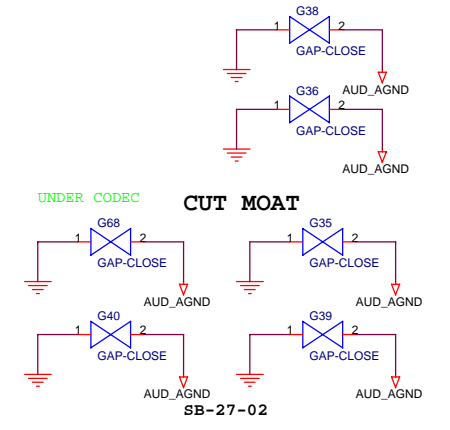
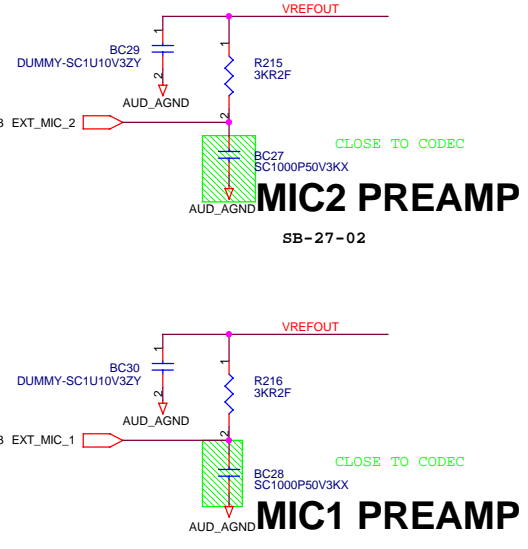
Cardbus I/F

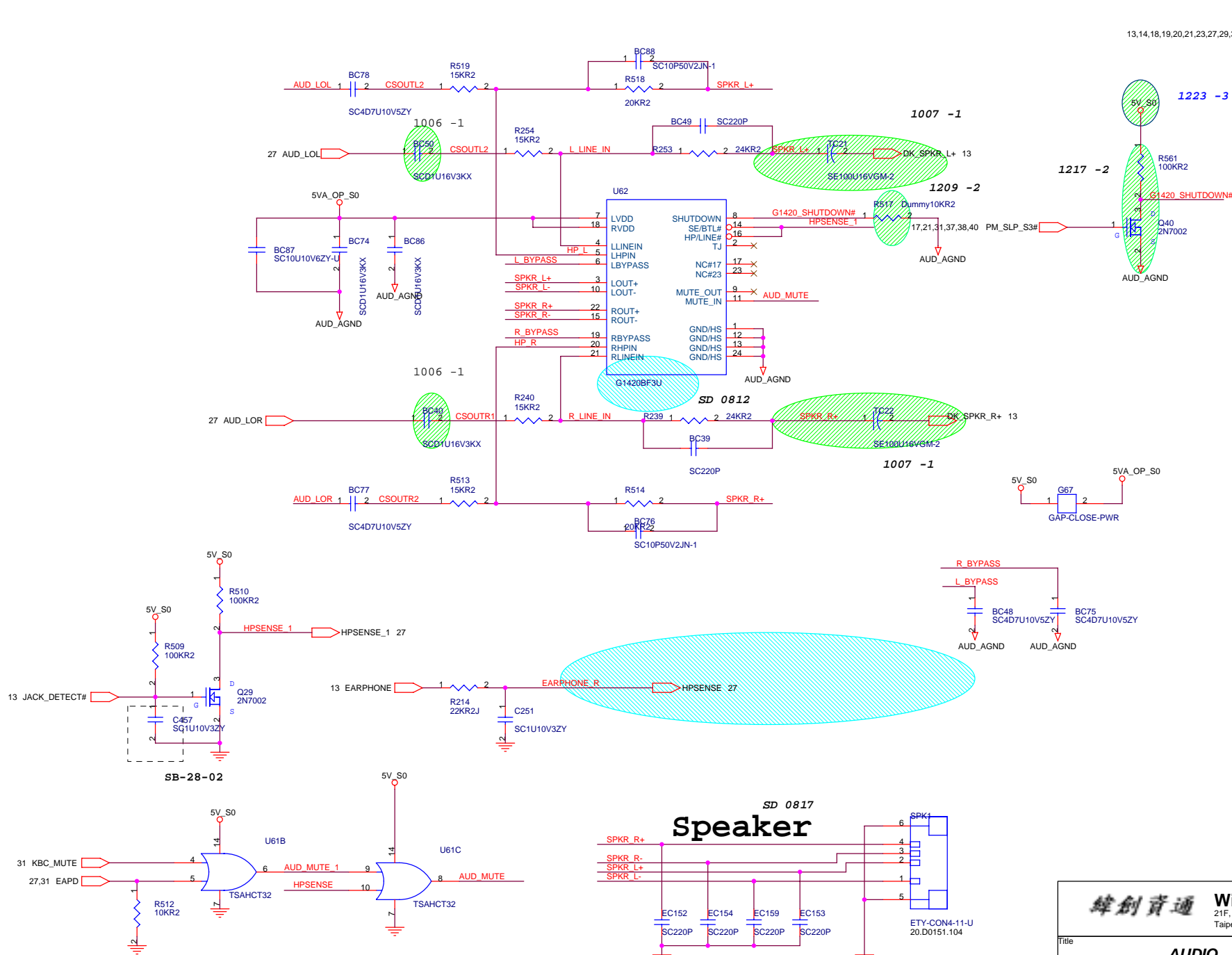


6 in 1 Connector

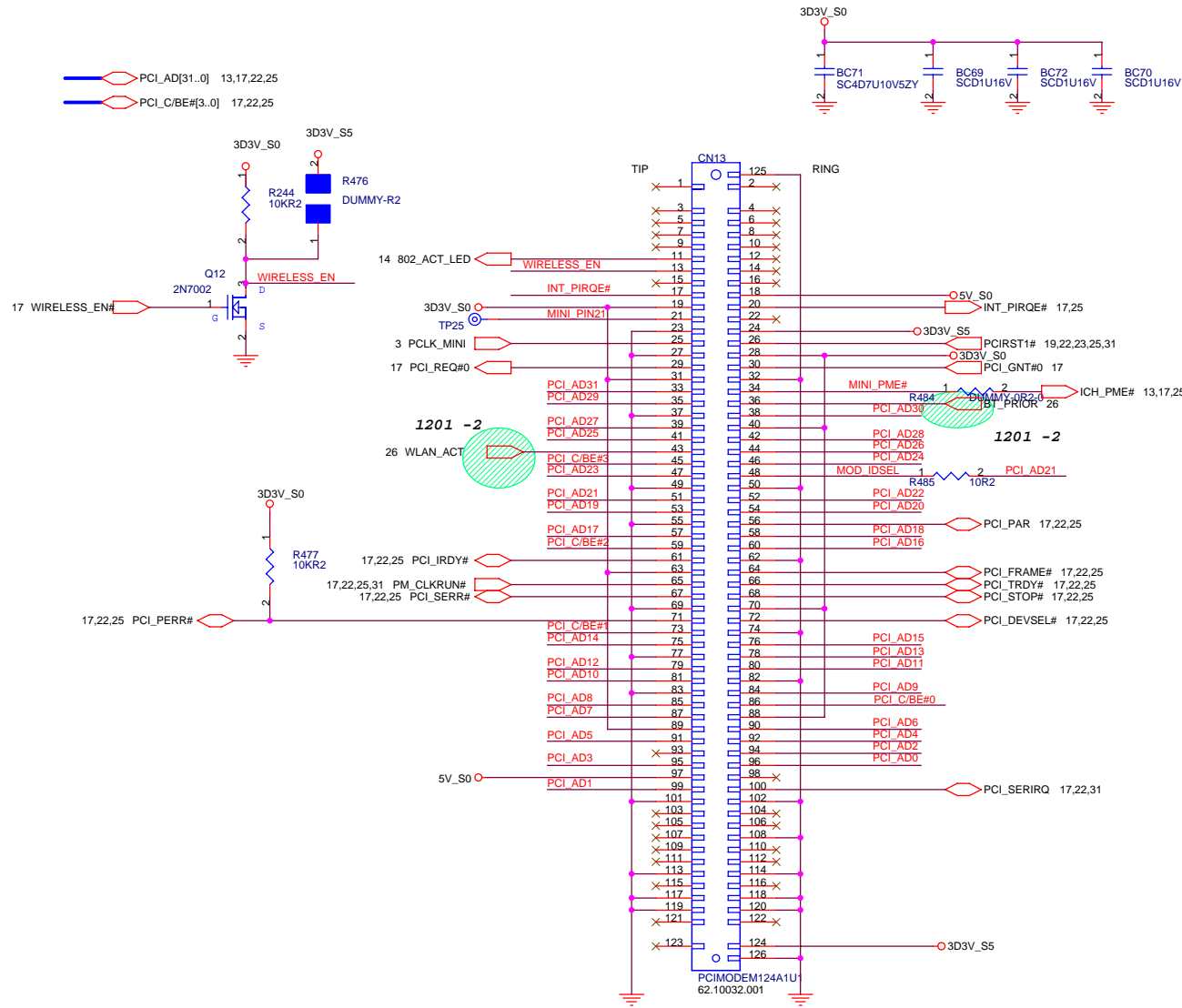


2/2 HM1-SB
ADI suggest

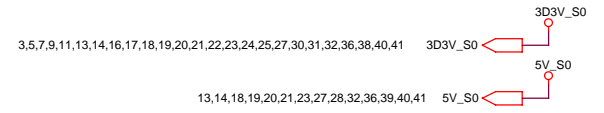




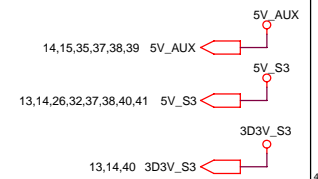
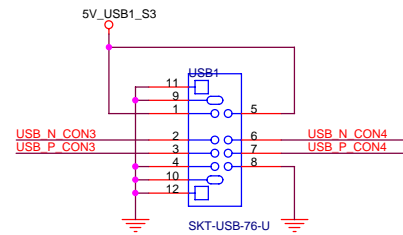
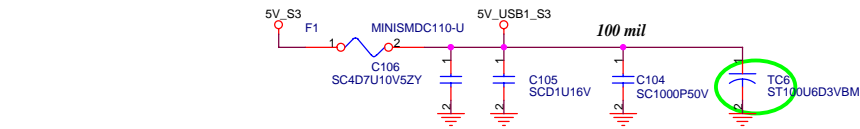
MINI-PCI



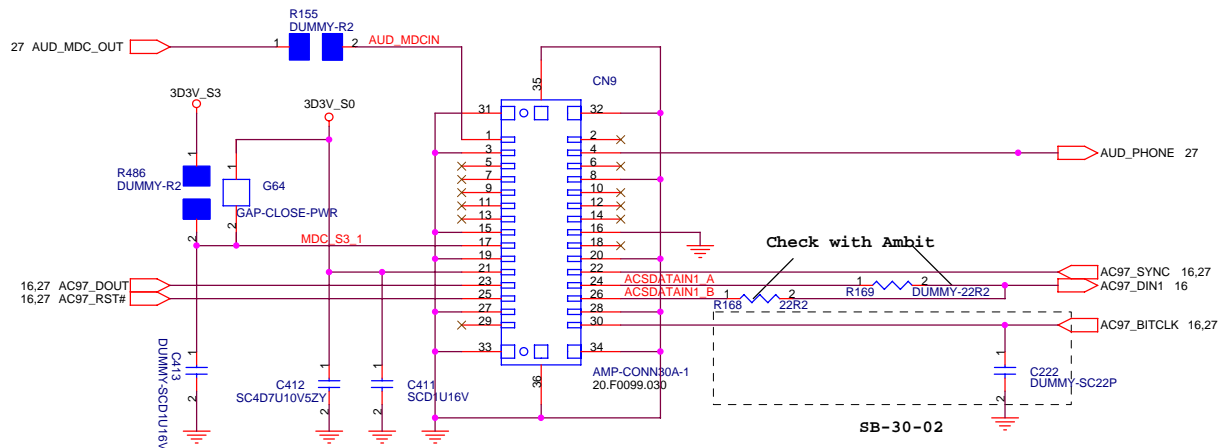
The symbol use 2nd source
The P/N is the main source
Main source:62.10032.001
2nd source:62.10032.031

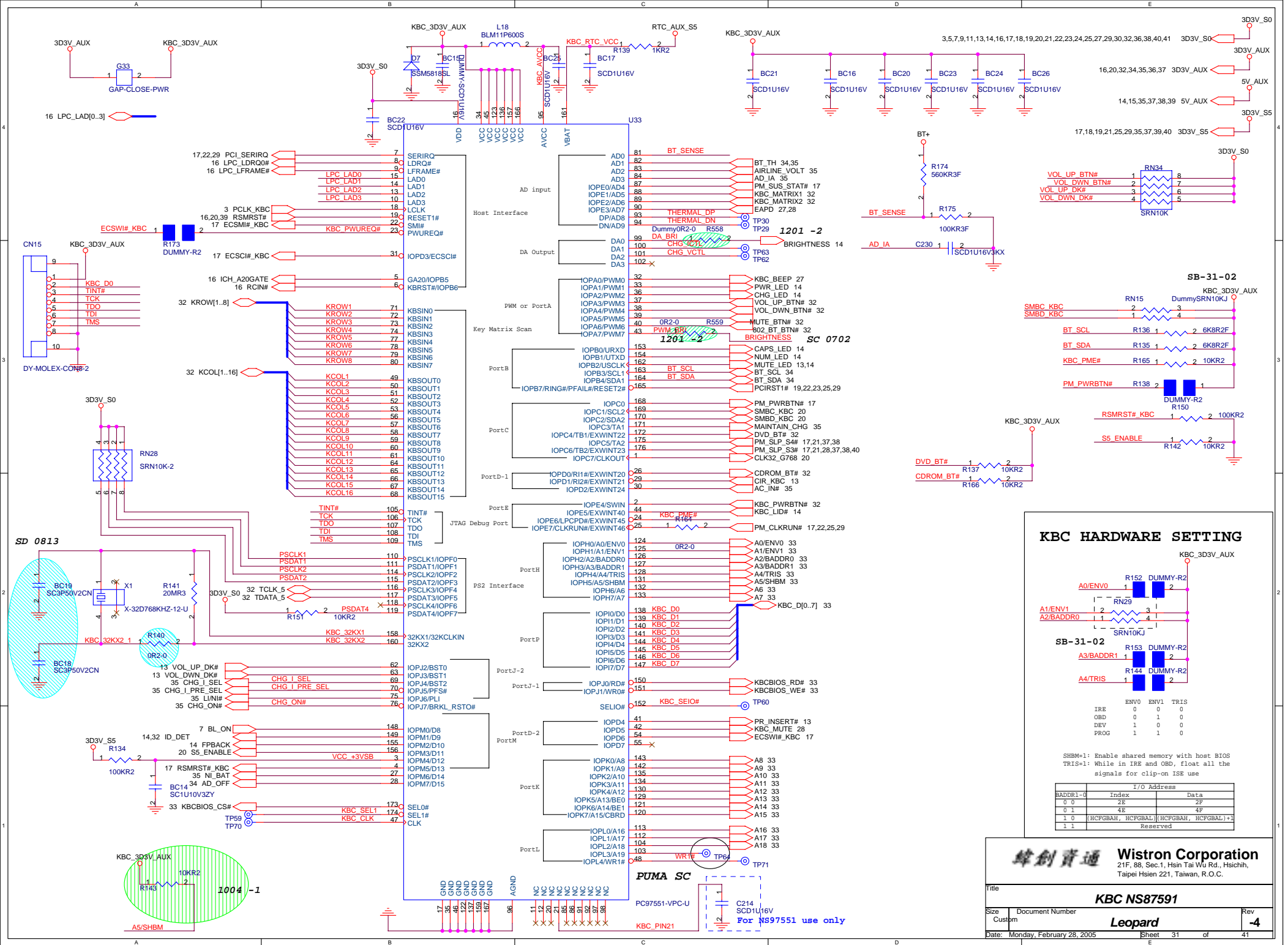


USB POWER



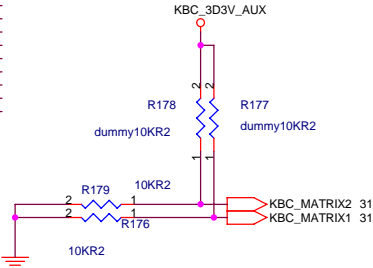
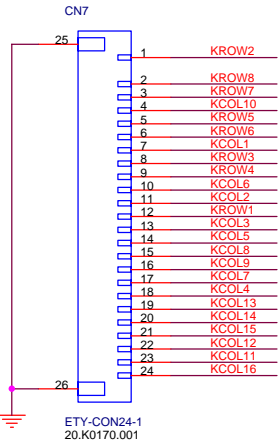
MDC Connector





INTERNAL KEYBOARD CONNECTOR

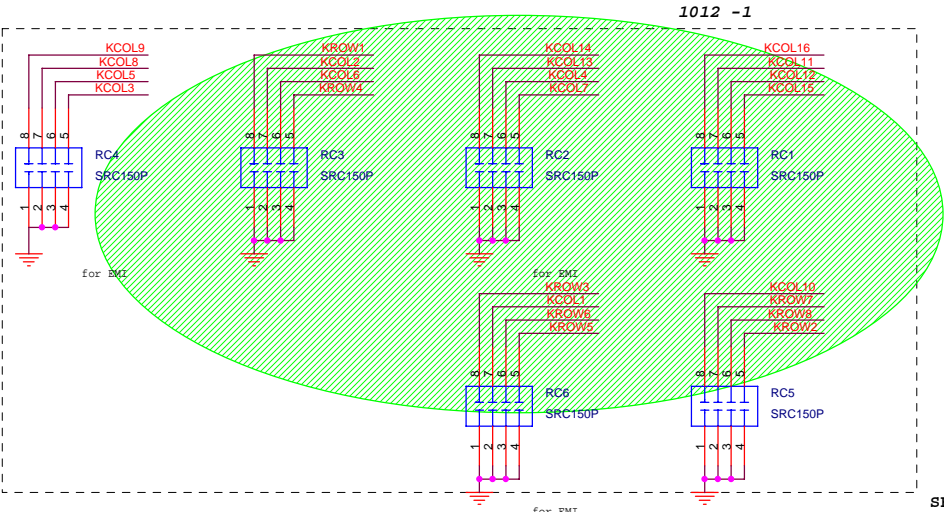
KROW[1..8] 31 KCOL[1..16] 31



the matrix table for PCB

KBC_MATRIX2, KBC_MATRIX1		
PA	PR	
FF	00	01
DF	10	11

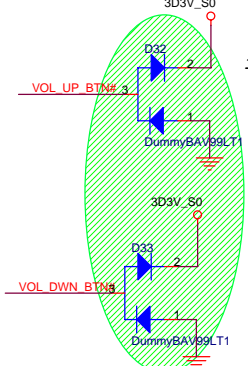
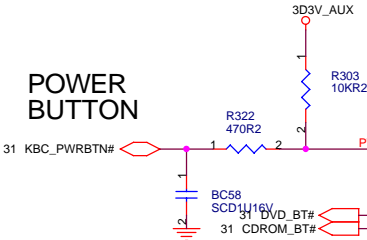
	NONE Quick Play	Quick Play
MATRIXID1#	0	1



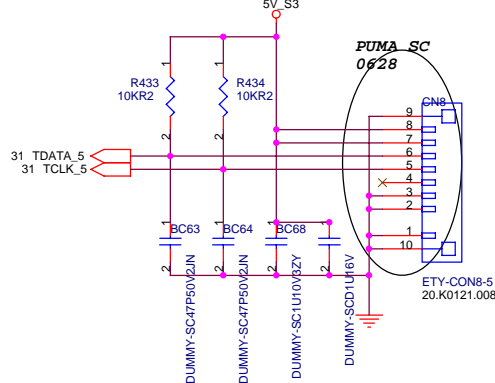
SB-32-01

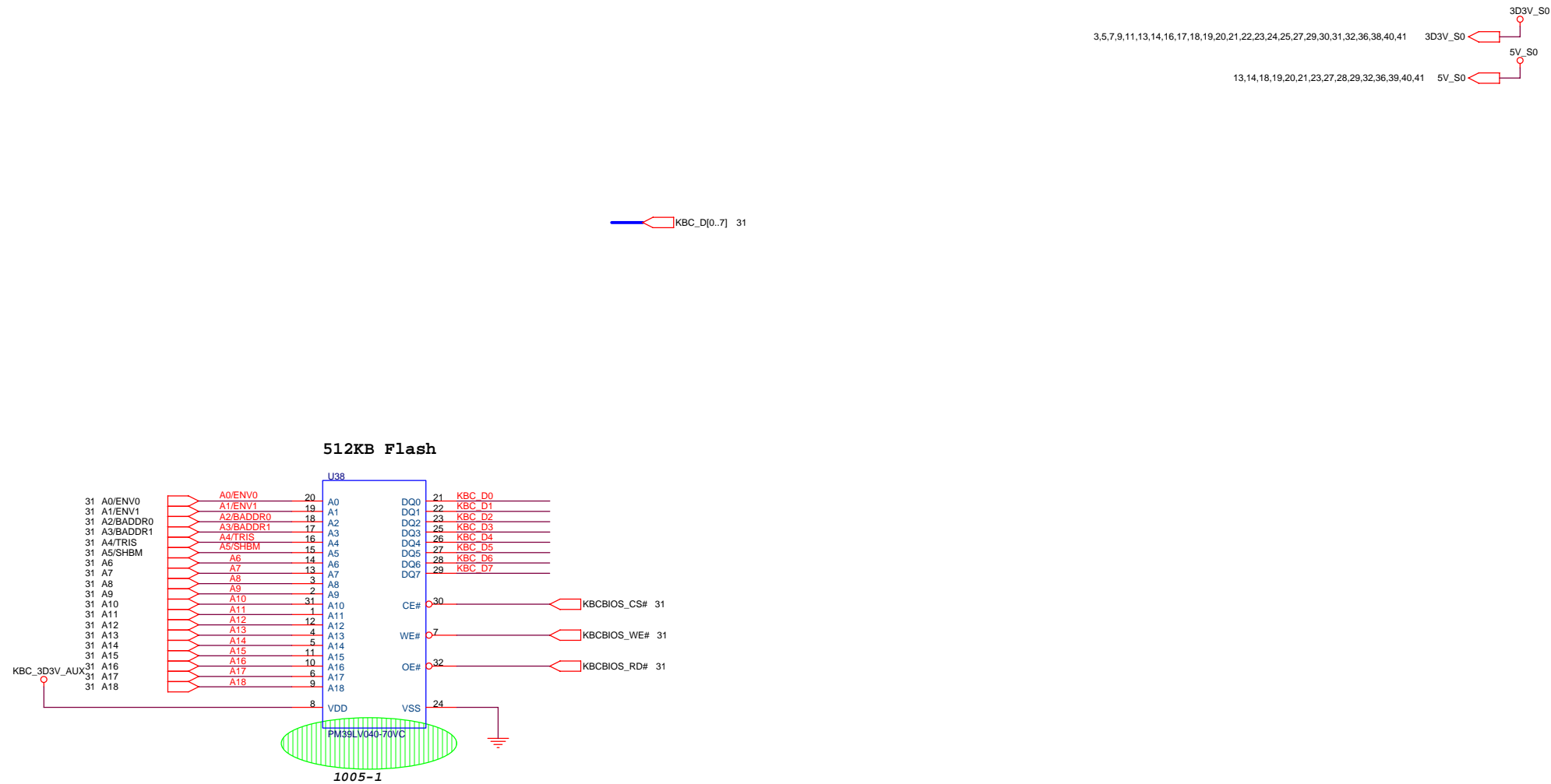
LAUNCH Board

POWER BUTTON



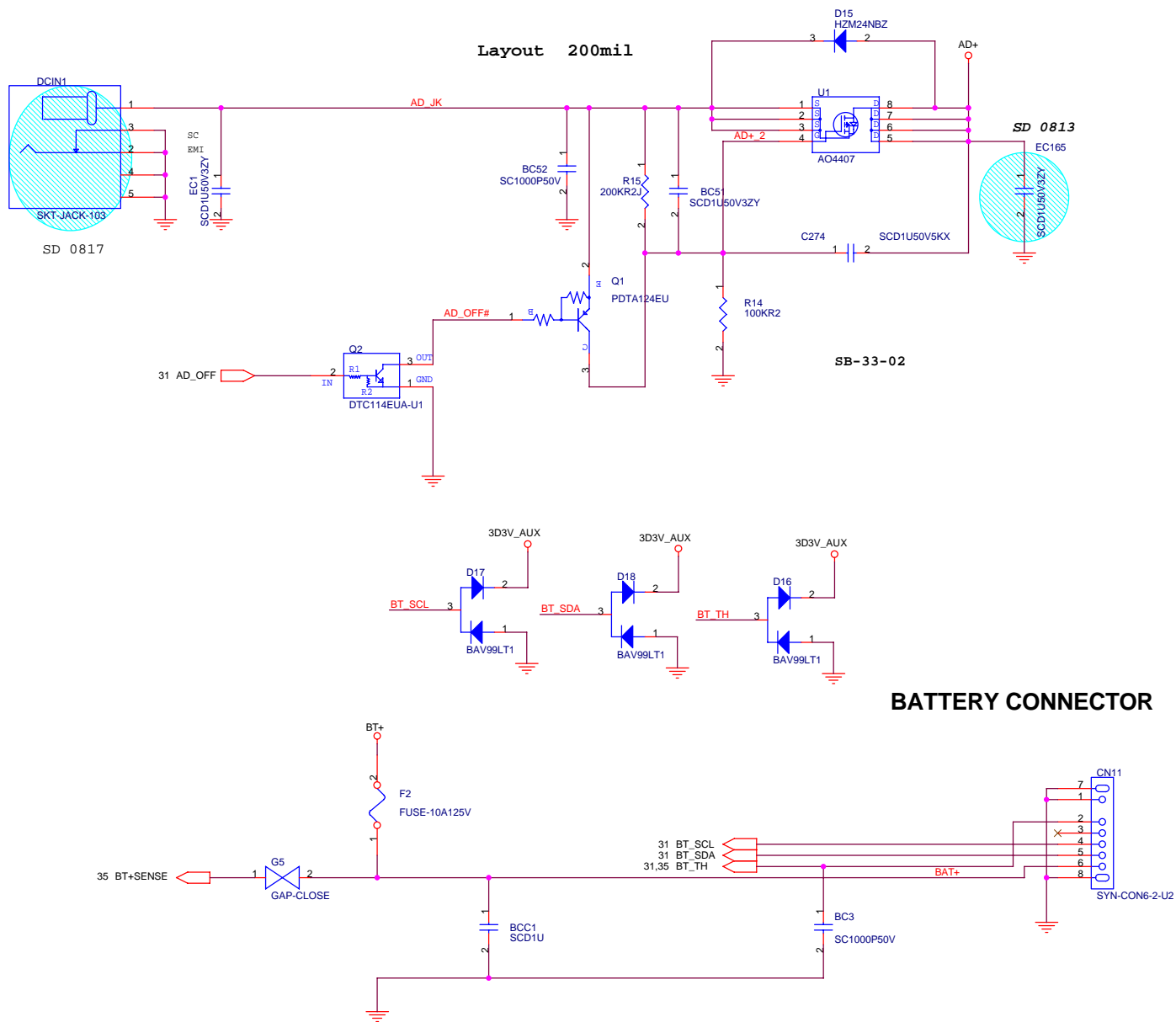
TouchPad Connector



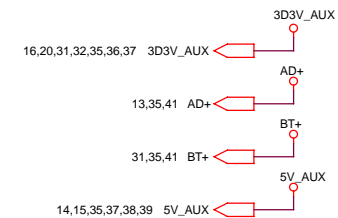


Adaptor in to generate DCBATOUT

Layout 200mil

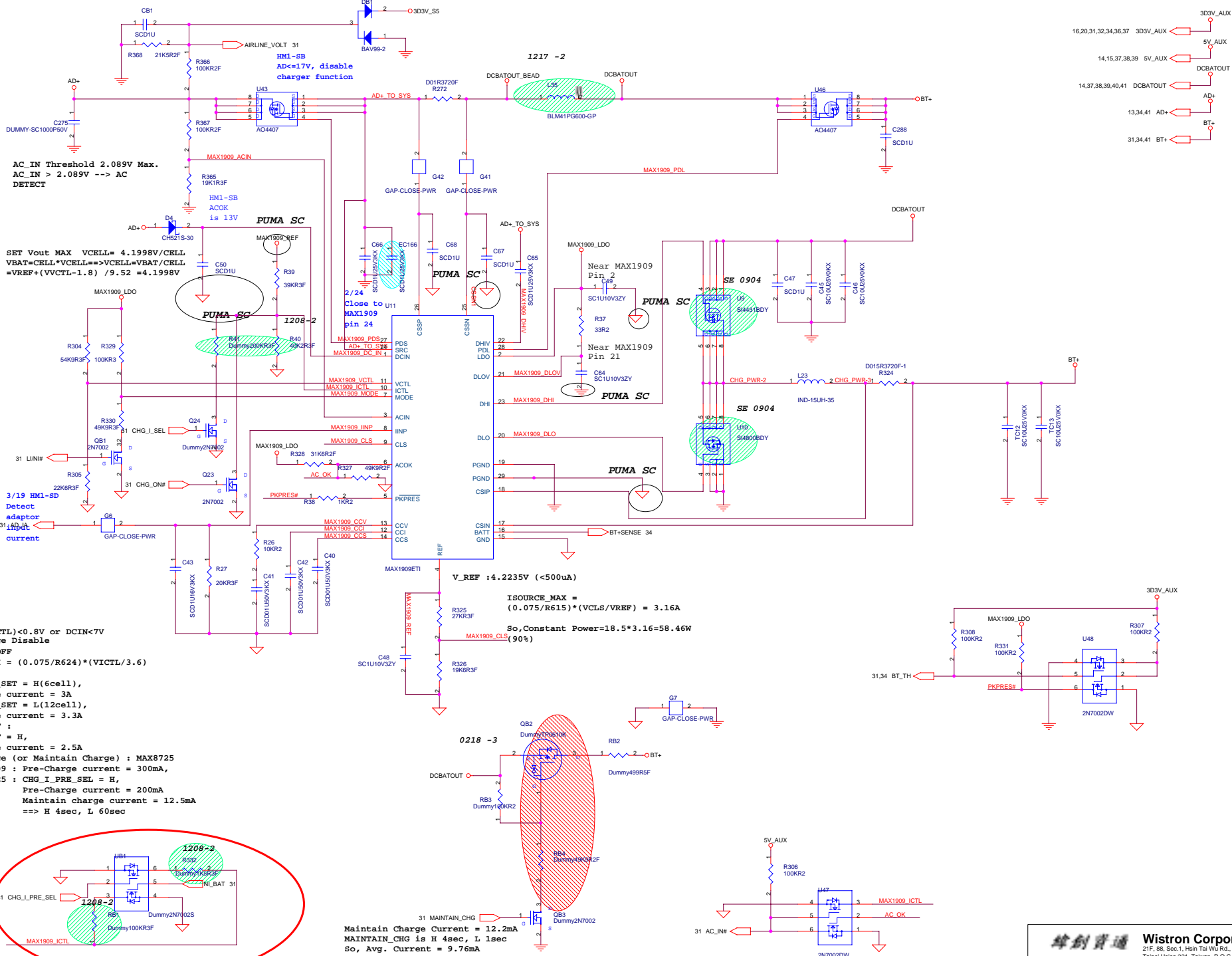


BATTERY CONNECTOR



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Adaptor/ Battery conn.	
Size	Document Number	Rev		
A3		Leopard		-4
Date: Monday, February 28, 2005		Sheet	34	of 41



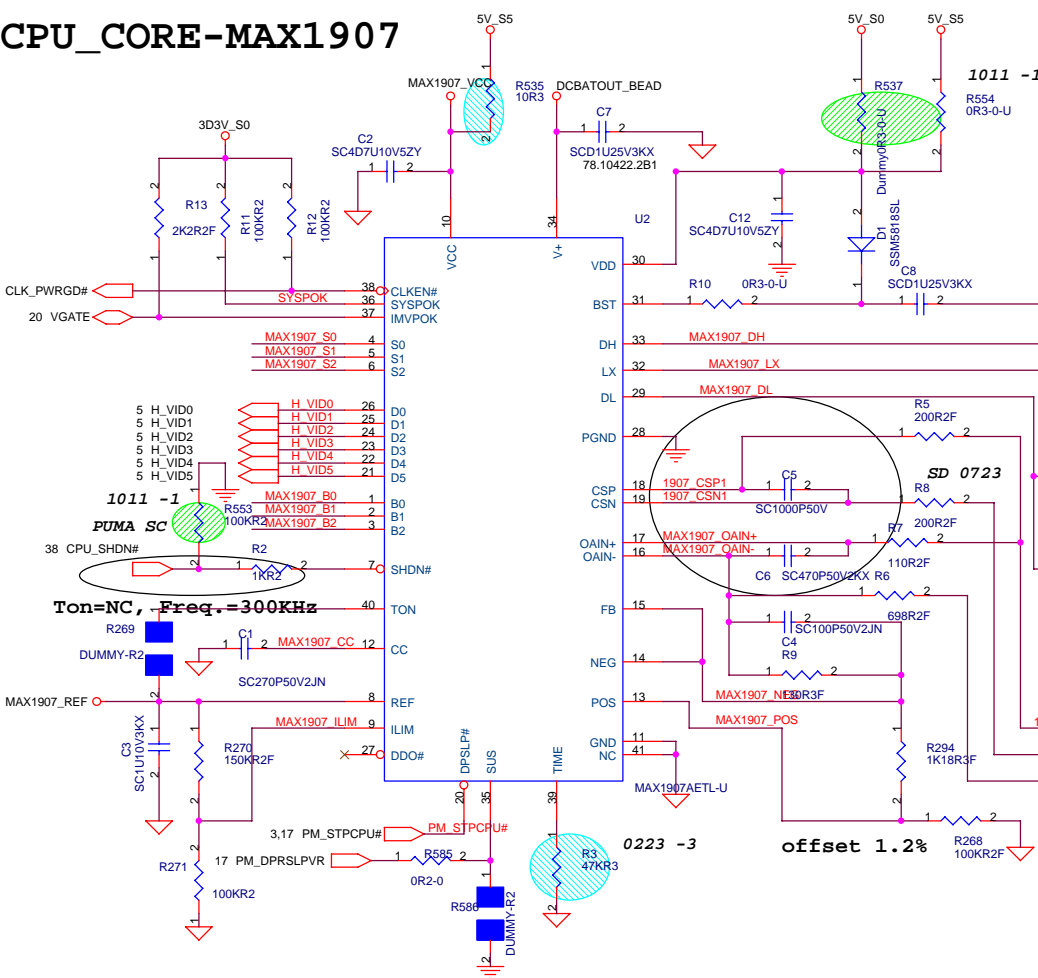
When V(ICTL)<0.8V or DCIN<7V
 -->Charge Disable
 SET CHG OFF
 $BAT_CHG_I = (0.075/R624) * (VICTL/3.6)$
 LI BAT :
 $CHG_I_SET = H(6cell),$
 Charge current = 3A
 $CHG_I_SET = L(12cell),$
 Charge current = 3.3A
 NI-MH BAT :
 $NI_BAT = H,$
 Charge current = 2.5A
 Pre-Charge (or Maintain Charge) : MAX8725
 MAX1909 : Pre-Charge current = 300mA,
 MAX8725 : $CHG_I_PRE_SEL = H,$
 Pre-Charge current = 200mA
 Maintain charge current = 12.5mA
 ==> H 4sec, L 60sec

Maintain Charge Current = 12.2mA
 MAINTAIN_CHG is H 4sec, L 1sec
 So, Avg. Current = 9.76mA

If Charger is MAX8725,dummy them.

If Charger is MAX1909,dummy them.

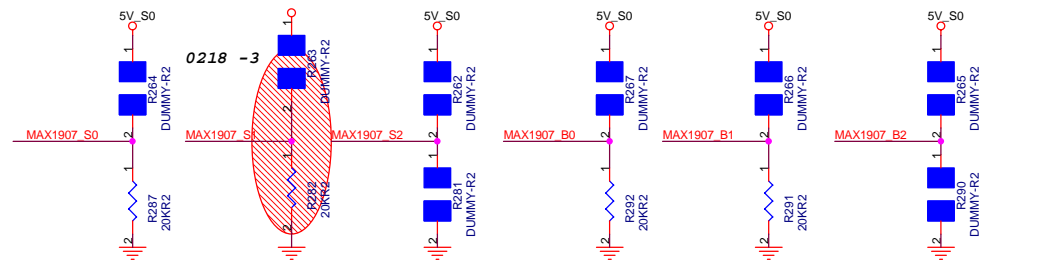
CPU_CORE-MAX1907



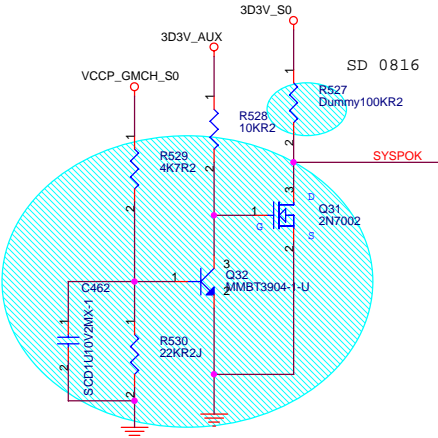
OCP=30A, Vally current = 27.5A,
Vilim=550mV(55mVp-p*10)

Deeper Sleep Voltage : 0.748V
, S0=L, S1=H, S2=Open,
5V_S0

Boot-up Voltage : 1.2V
, B0=L, B1=L, B2=Open



VID							Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V	
0	1	0	1	1	1	1.340	
0	1	1	0	0	0	1.324	
0	1	1	0	1	0	1.292	
0	1	1	1	0	0	1.260	
0	1	1	1	0	1	1.244	
0	1	1	1	1	1	1.212	
1	0	0	0	0	1	1.180	
1	0	0	0	1	1	1.148	
1	0	0	1	1	0	1.100	
1	0	1	0	0	1	1.052	
1	0	1	0	1	1	1.020	
1	0	1	1	1	0	0.972	
1	1	0	0	0	0	0.940	



SYSTEM DC/DC 3D3V_S5 / 5V_S5

3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41 3D3V_S0
 17,18,19,21,25,29,31,35,39,40 3D3V_S5
 16,20,31,32,34,35,36 3D3V_AUX
 14,18,20,36,38 5V_S5
 14,15,35,38,39 5V_AUX
 14,35,38,39,40,41 DCBATOUT

3V = 4Arms,
 OCP>6A

5V = 5Arms,
 OCP>6.8A

These components should be
 located near by MAX1977

These components should be
 located near by MAX1977

ILIM5: $5V * 200K / (200K + 300K) = 2.0V$
 $200mV / 24 = 8.3A$
 OCP point = $8.3A + 1/2Ripple$

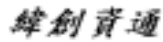
ILIM3: $5V * 200K / (200K + 300K) = 2.0V$
 $200mV / 24 = 8.3A$
 OCP point = $8.3A + 1/2Ripple$
 OCP point = $20A + 1/2Ripple$

ILIM*=Vcc 100mV
 ILIM*=Vref 200mV
 OCP= $0.1Vth/Rds(on) + 0.5Ripple$

5V_S5 spec. = 10mA

SKIP# > 2.4V : PWM mode
 SKIP# = GND(0.8V) : SKIP MODE
 SKIP# = REF (1.7V-2.3V)/Floating
 Ultrasonic MODE(25KHz min)

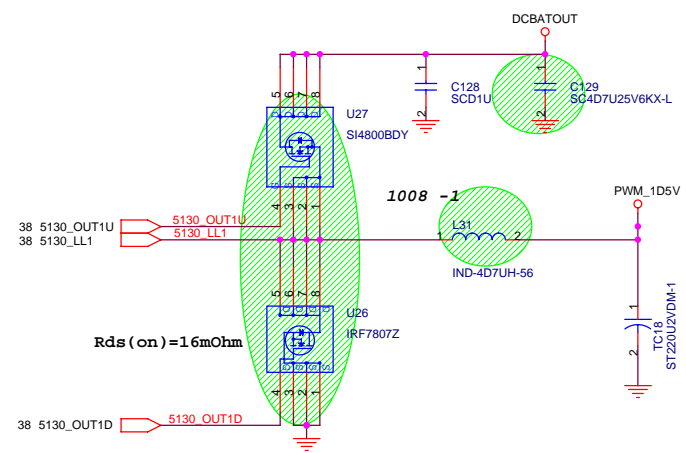
PM_SLP_S3# high = PWM
 PM_SLP_S3# low = Ultrasonic

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title DC/DC 3V_S5/5V_S5	
Size A3	Document Number Leopard
Date: Monday, February 28, 2005	Rev -4
Sheet 37	of 41

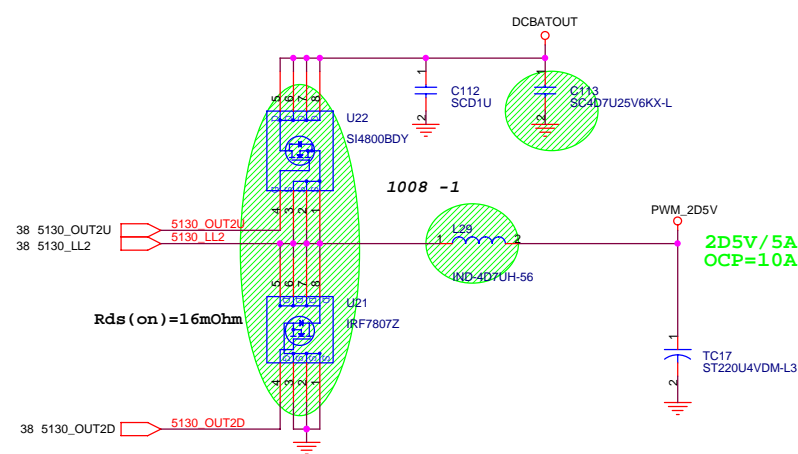
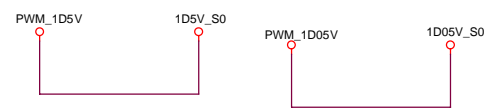
(1D5V=>CH1 , 2D5V=>CH2 , 1D05V =>CH3)



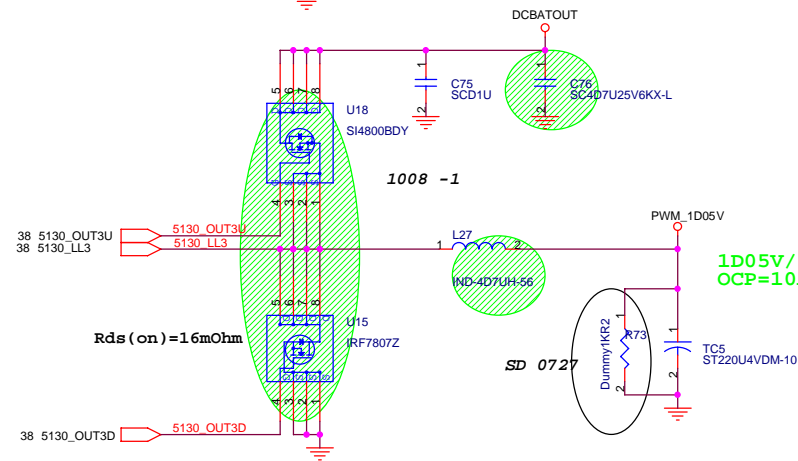
TI TPS5130 for 2.5V, 1.5V, 1.05V
(1D5V=>CH1 , 2D5V=>CH2 , 1D05V =>CH3)



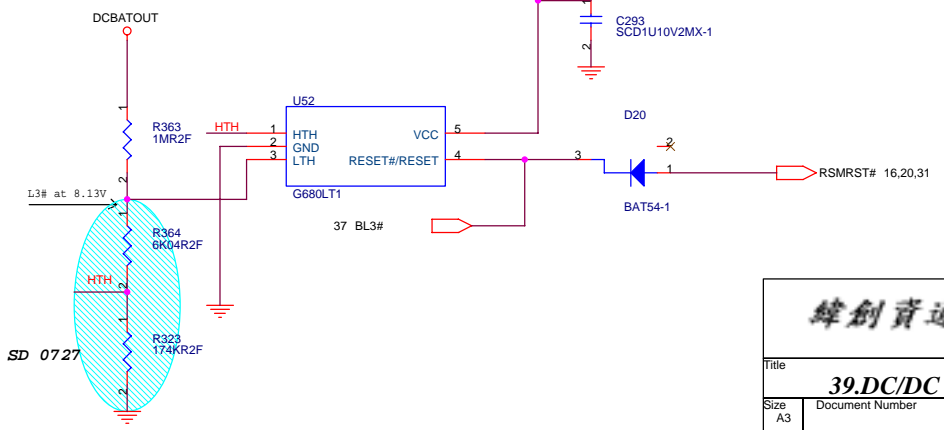
1D5V/5A
OCP=10A



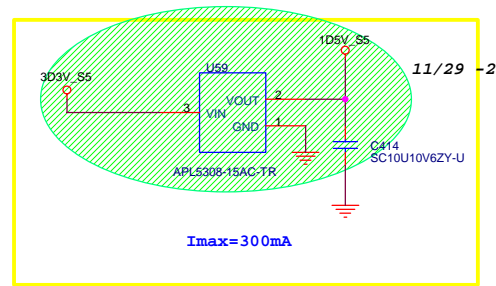
2D5V/5A
OCP=10A



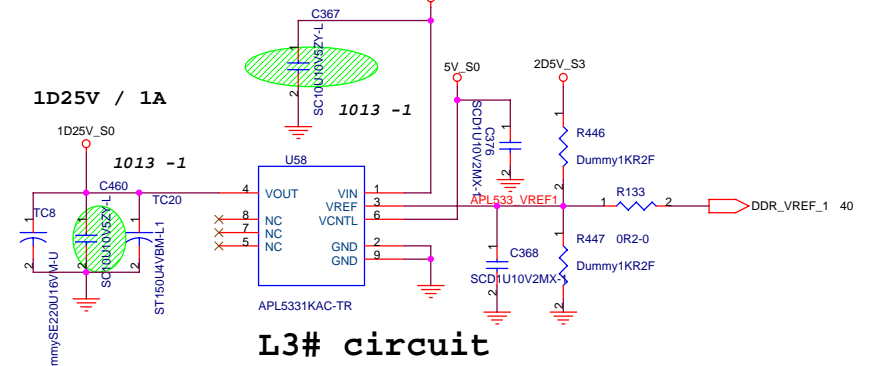
1D05V/5A
OCP=10A



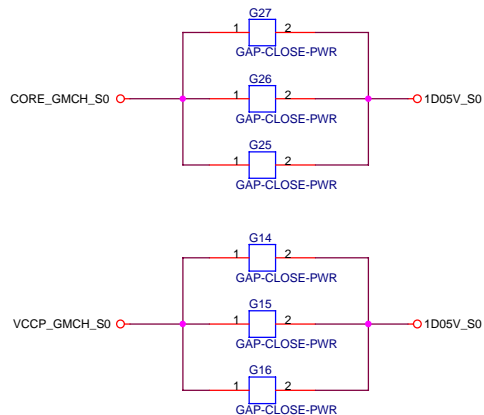
1.5V_S5 (For ICH6)



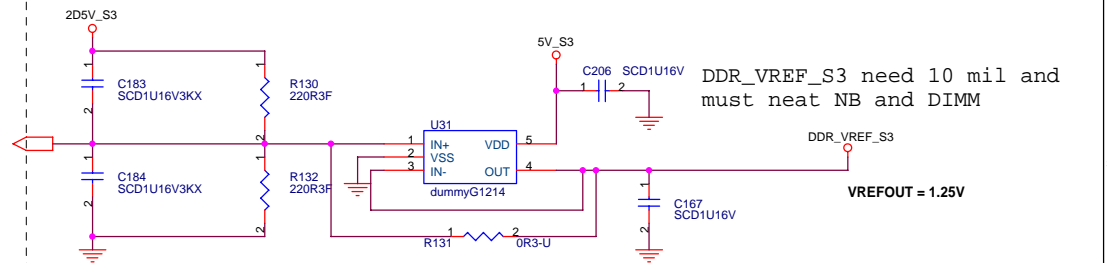
Power budget: 1.25V/2.2Apeak (For DDR1_VTT)



FOR GMCH Power



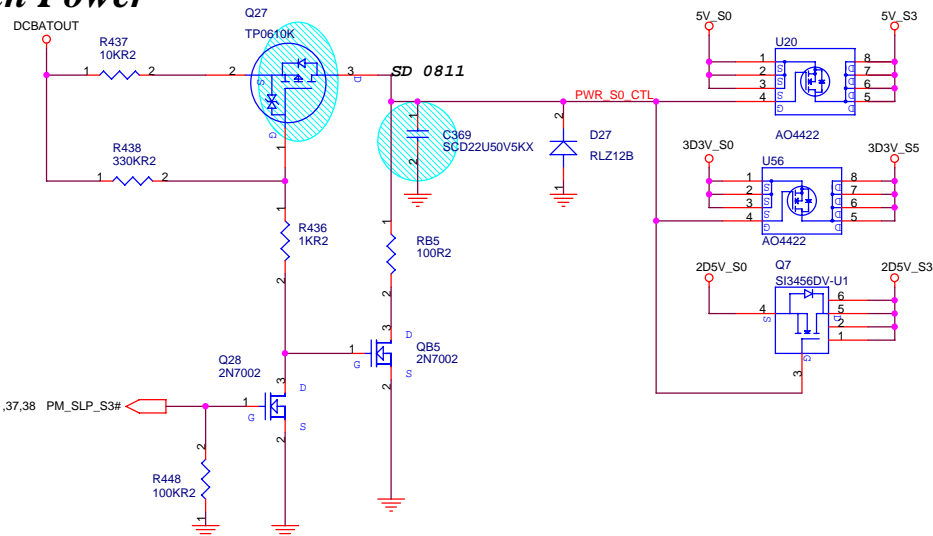
39 DDR_VREF_1



FOR DDR Power

Run Power

0223 -3



Suspend Power



