

# GENEVA

CPU : MEROM  
Chip Set : SANTAROSA CHIPSET  
Remarks : Mobility Platform

Model Name : GENEVA  
PBA Name : MAIN  
PCB Code : BA41-XXXXX  
Dev. Step : PV2  
Revision : 1.0  
T.R. Date :

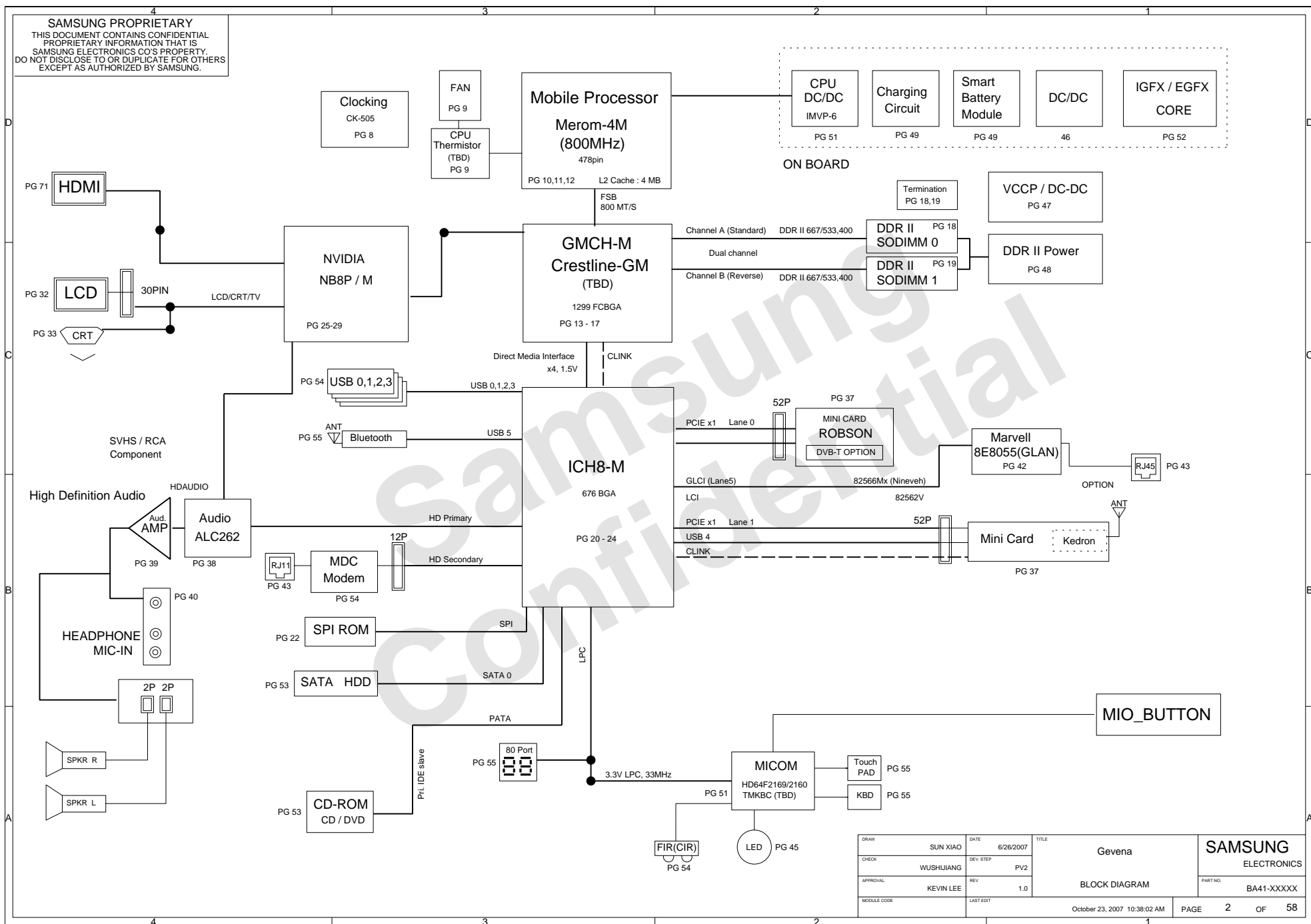
DRAW	CHECK	APPROVAL

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DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva	SAMSUNG ELECTRONICS
CHECK	WUSHUIJANG	DEV. STEP	PV2	MILAN	PART NO.	
APPROVAL	KEVIN LEE	REV	1.0	COVER	BA41-XXXXX	
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DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS PART NO. BA41-XXXXX
CHECK	WUSHUJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0		BLOCK DIAGRAM	
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## BOARD INFORMATION

### SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

#### PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	B,C,D
DT PCI SLOT	AD22	1	B,C,D,C
MiniPCI SLOT	AD23	2	A,B
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

#### Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core Voltage for CPU
MCH_CORE	Core Voltage for CPU
ICH1_CORE	Core Voltage for CPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH8-M
P1.05V_M	1.05V switched power rail for ME (on in M0/M1)
P1.25V_M	1.25V switched power rail for ME (on in M0/M1)
P3.3V_M	3.3V switched power rail for ME (on in M0/M1)
P3.3V_A	3.3V always power rail (by KBC3_ALWS_ON)
MICOM_P3V	3.3V always power rail (for Micom)
LAN_3.3V	3.3V always power rail (for LAN)
P1.5V	1.5V switched off power rail (off in S3-S5)
P1.5V_AUX	1.5V switched on power rail
P2.5V	2.5V switched off power rail (off in S3-S5)
P1.8V	1.8V switched off power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR
P0.9V	0.9V power rail for DDR
P3.3V	3.3V switched off power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail
PSV	5.0V switched off power rail (off in S3-S5)
PSV_AUX	5.0V switched on power rail

#### USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	DMB
3	Expresas Card
4	DOCKING PORT 0
5	Bluetooth
6	Mini PCI Express
7	Aux Display
8	Test Port (RSVD)
9	WWAN/WIBRO (TBD)

#### PCI Express Assign

PORT #	ASSIGNED TO
0	PCI-E x1 Slot
1	Mini Card (Golan)
2	Mini Card (WIBRO : RSVD)
3	Expresas Card
4	DOCKING PORT 0
5	GLAN

#### Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH8-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	24.576MHz	Cardbus Controller	1394
Crystal	25MHz	LAN	Intel LAN
Crystal	27MHz (TBD)	VIDEO	PEG
Crystal	24.576MHz (TBD)	HD Audio	Audio

#### LCD Pannel Detect

(TBD)

Devices	Resolution	PANNEL_DETECT_0

#### I<sup>2</sup>C / SMB Address

Devices	Address	Hex	Bus
ICH8-m	Master	-	SMBUS Master
CPU Thermal Sensor	1001 110x	9Ch	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
DB400 (PCI Express Clocks)	1101 110x	DCh	Clock Buffer for PCI Express
TBD	0100 1100	4Ch	Thermal Sensor
TBD : (LVDS BackLight Inverter)	0101 1000	58h	-
TBD : (ALS)	0111 0010	72h	Ambient Light Sensor
TBD : (AUX DISPLAY)	0011 110x	3Ch	EMA
LAN	1100 1000	C8h	82566
PCI Express Docking	TBD	TBD	TBD
TPM	TBD	TBD	TBD

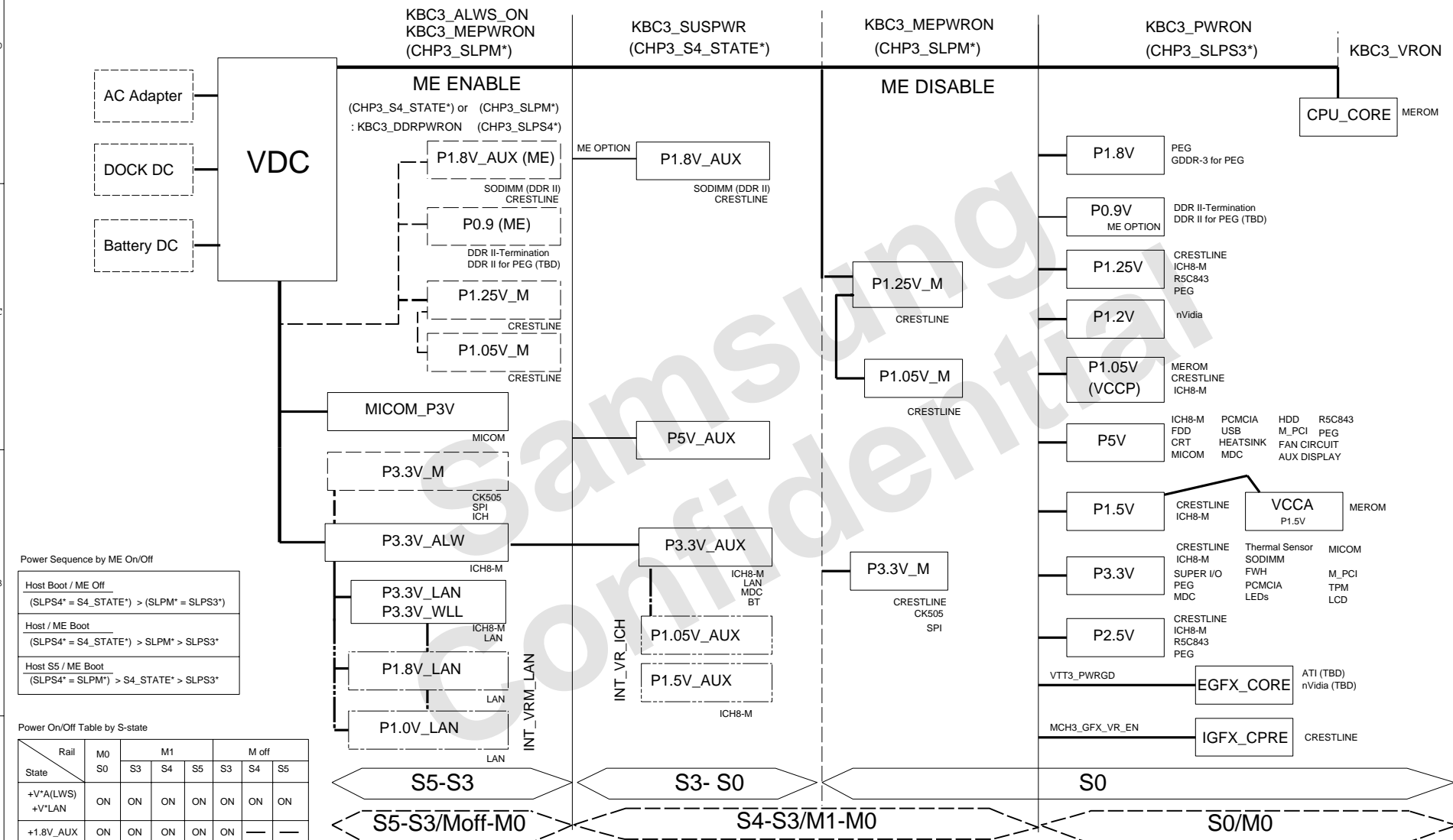
### REVISION HISTORY

See rev notes for more information.

DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHUJIANG	DEV. STEP	PV2			ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0	BOARD INFO		PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE 3 OF 58	

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# POWER DIAGRAM

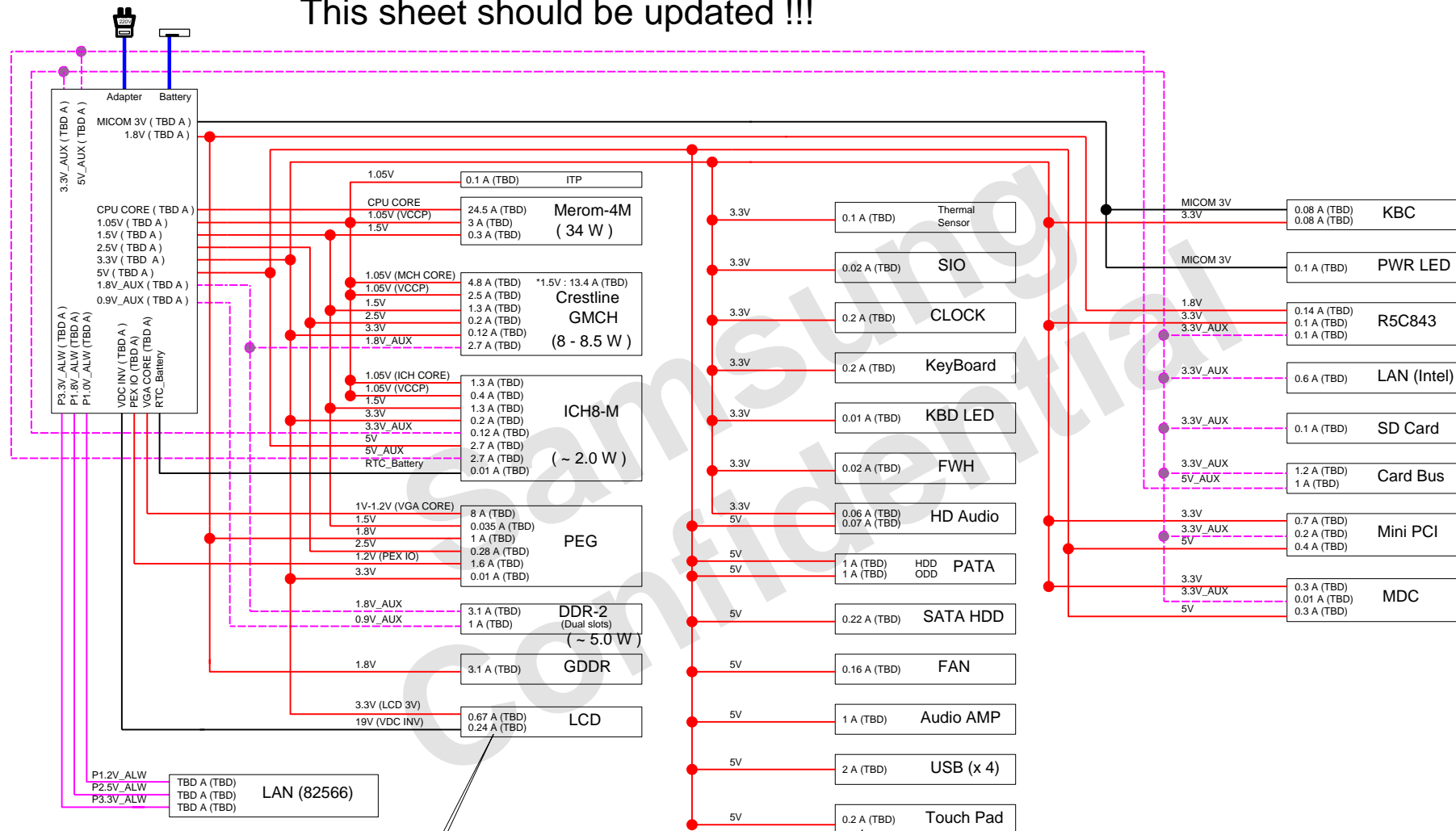


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# POWER RAILS ANALYSIS

Rev. 0.5

This sheet should be updated !!!



Value by Datasheet/Application notes (Value by measurement)

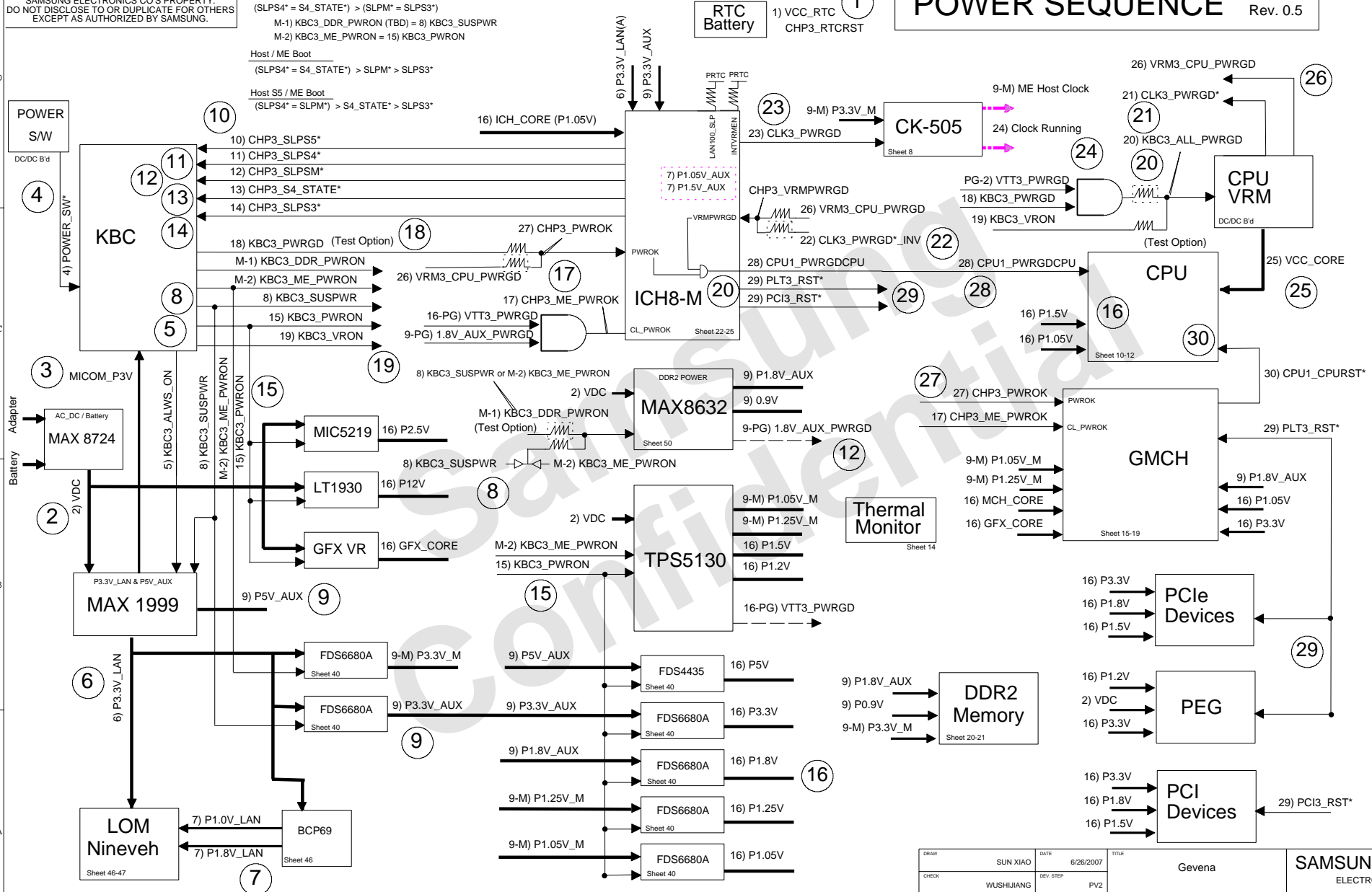
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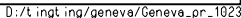
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TO BE UPDATED!!

# POWER SEQUENCE

Rev. 0.5



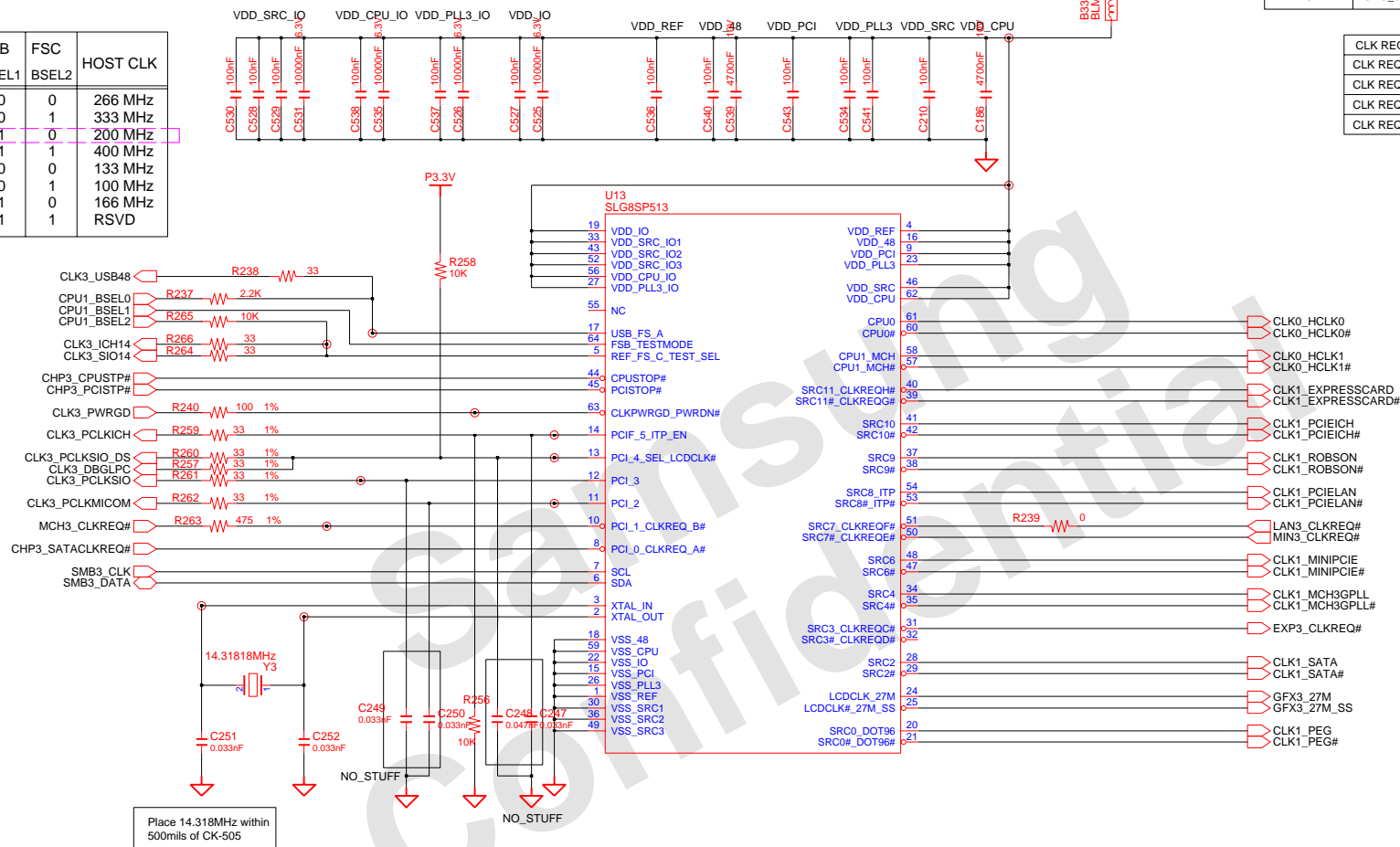


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FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

SEL_LCDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	LCDCLK/LCDCLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

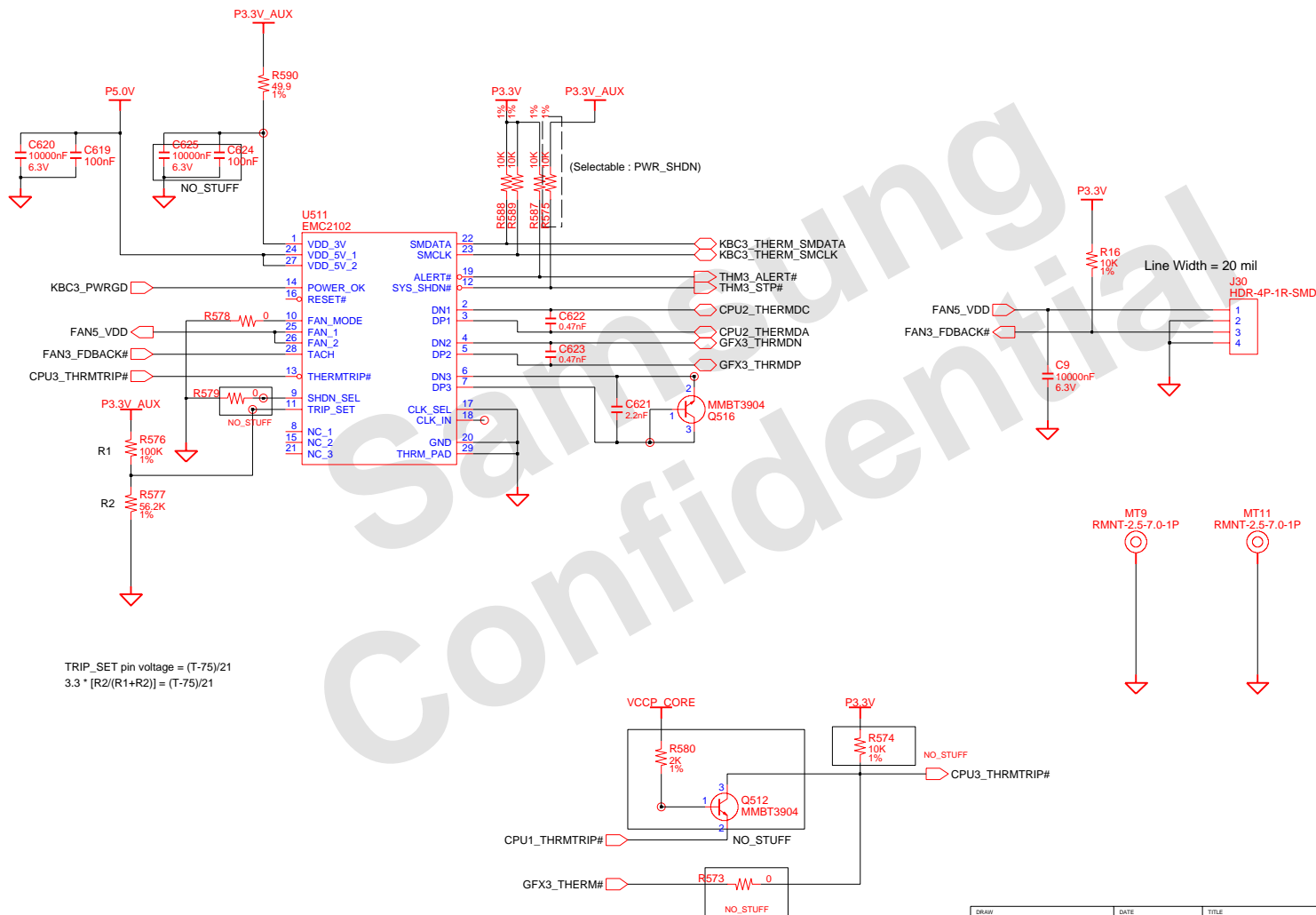
CLK REQ	DEVICE	SRC POR
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXPRESS CARD	SRC8



DRAW	SUN XIAO	DATE	6/26/2007	Gevena CLOCK GENERATOR CK-505		SAMSUNG ELECTRONICS		
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APPROVAL	KEVIN LEE	REV	1.0					
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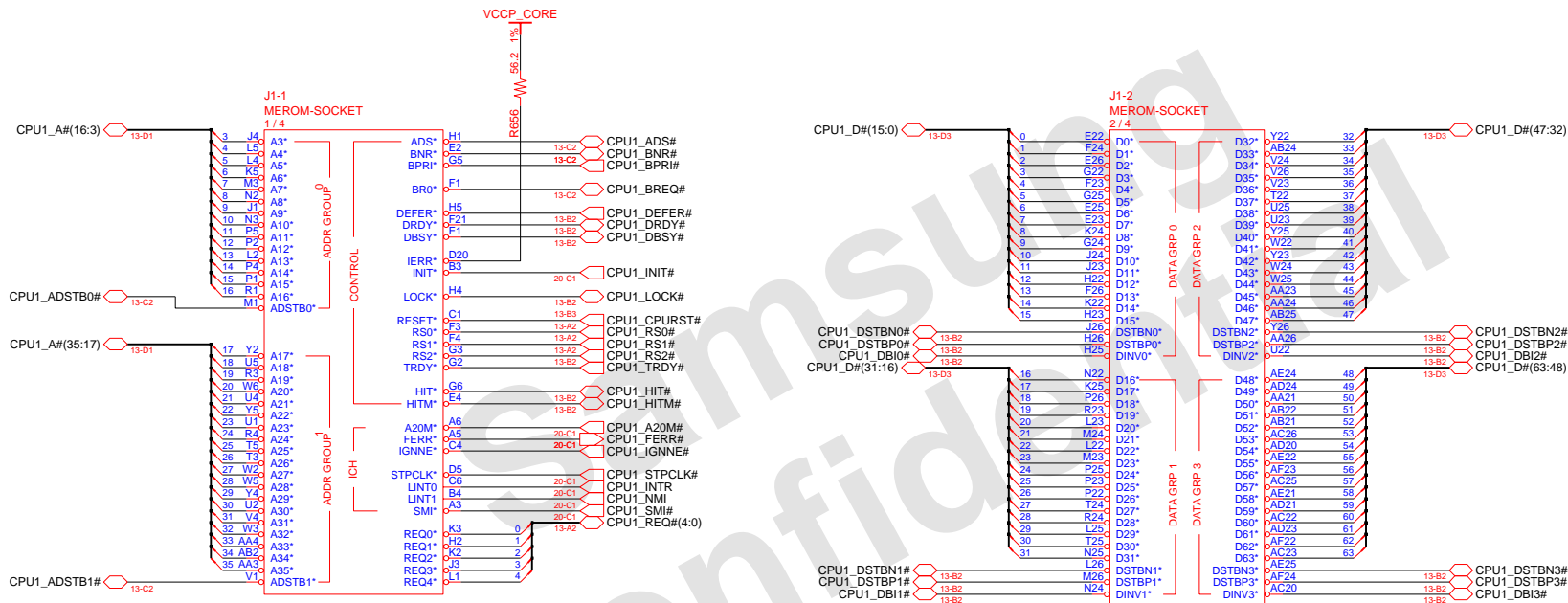


# THERMAL SENSOR & FAN CONTROL



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena THERMAL BLOCK THERMAL & FAN CONTROL	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2			PART NO. BA41-XXXXX
APPROVAL	KEVIN LEE	REV	1.0			
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CPU CONNECTOR PART NUMBER 3704-001153

DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena CPU MEROM(1/3)	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2			PART NO. BA41-XXXXX
APPROVAL	KEVIN LEE	REV	1.0			
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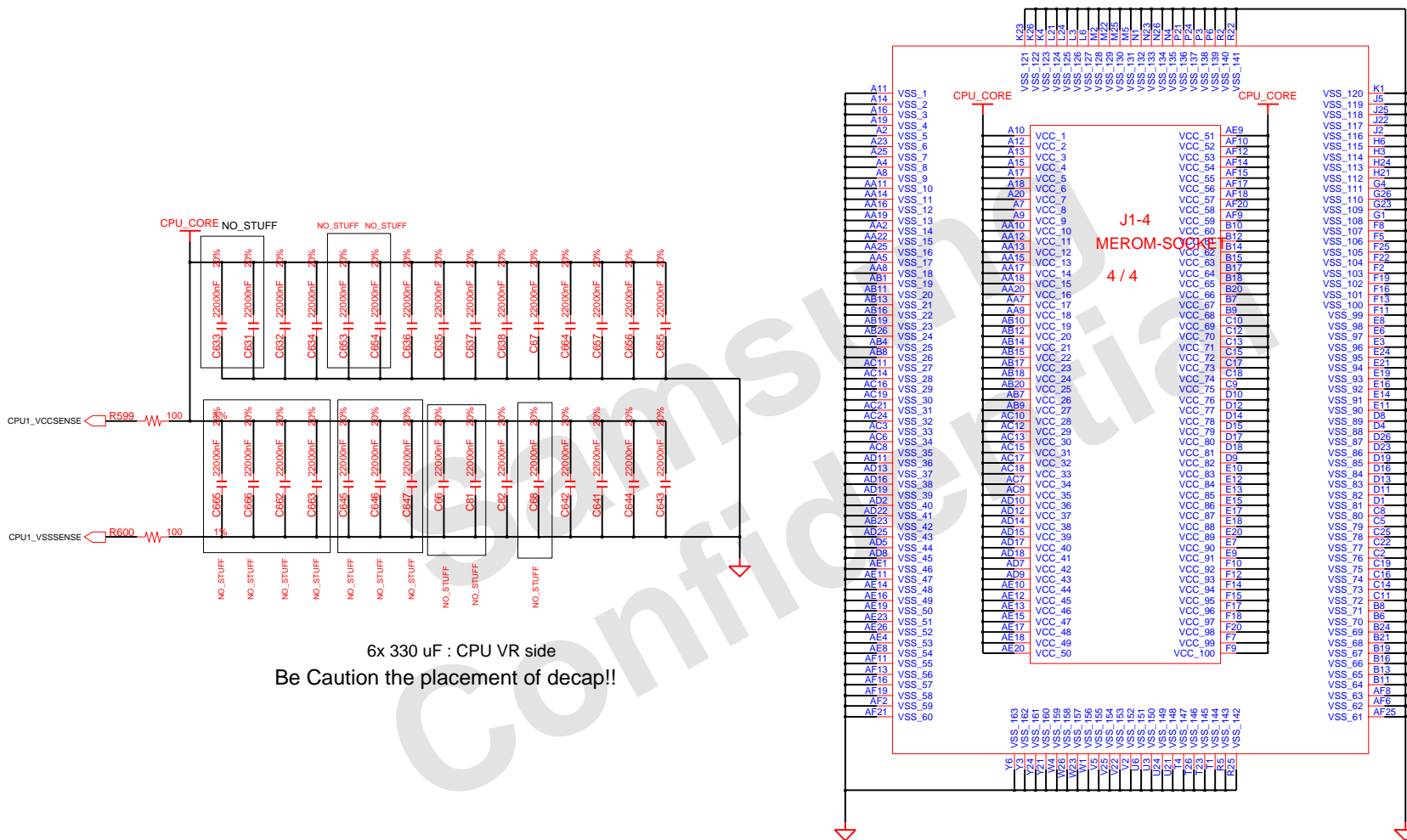
IMVP-6

\*Yonah Processor (2.33 GHz / 800 MHz : TBD)

GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a  $Z_0=55\text{ohm}$  traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

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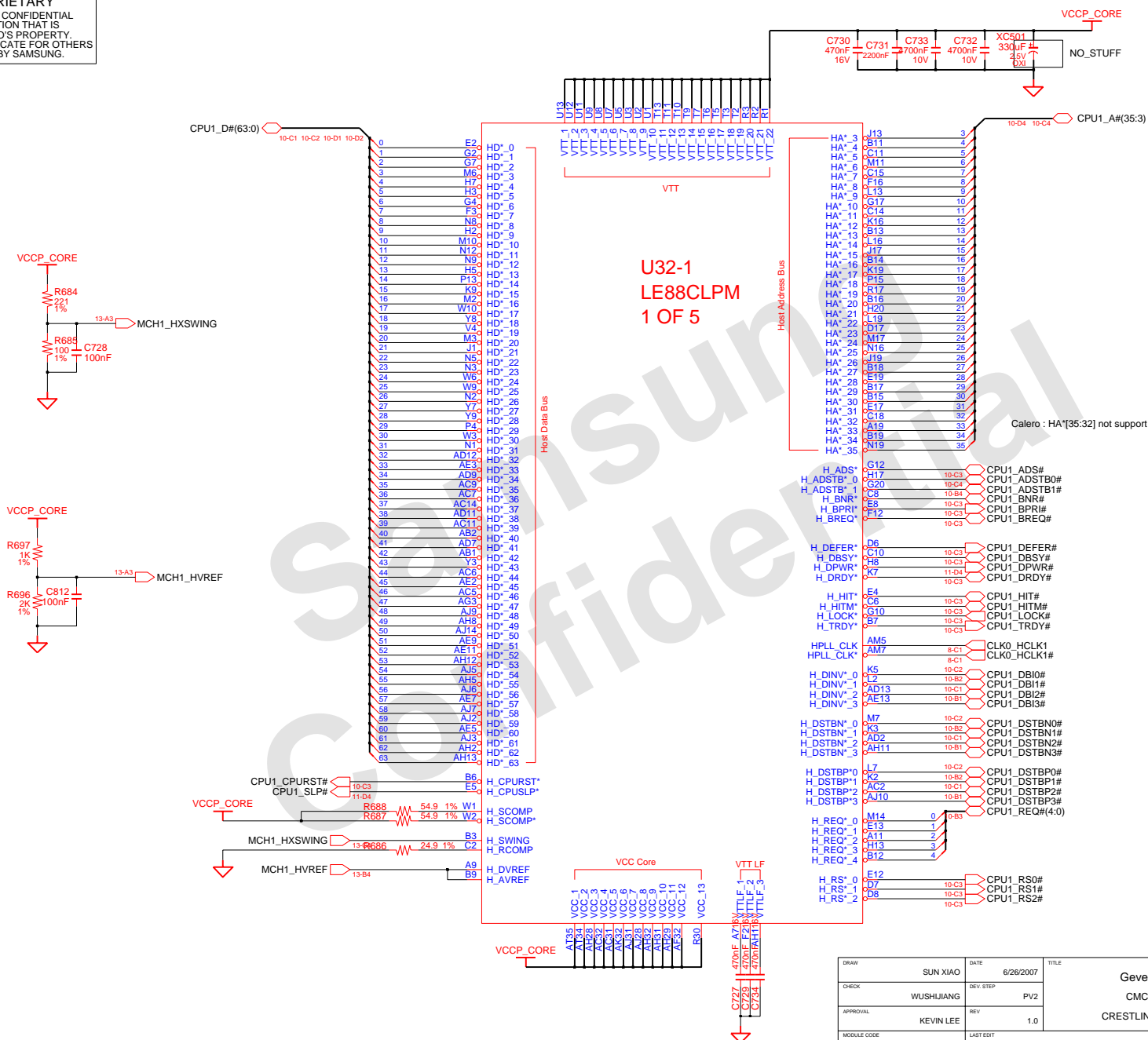
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CHECK	WUSHUJIANG	DEV. STEP	PV2		CPU
APPROVAL	KEVIN LEE	REV	1.0		MEROM(3/3)
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	12 OF 58

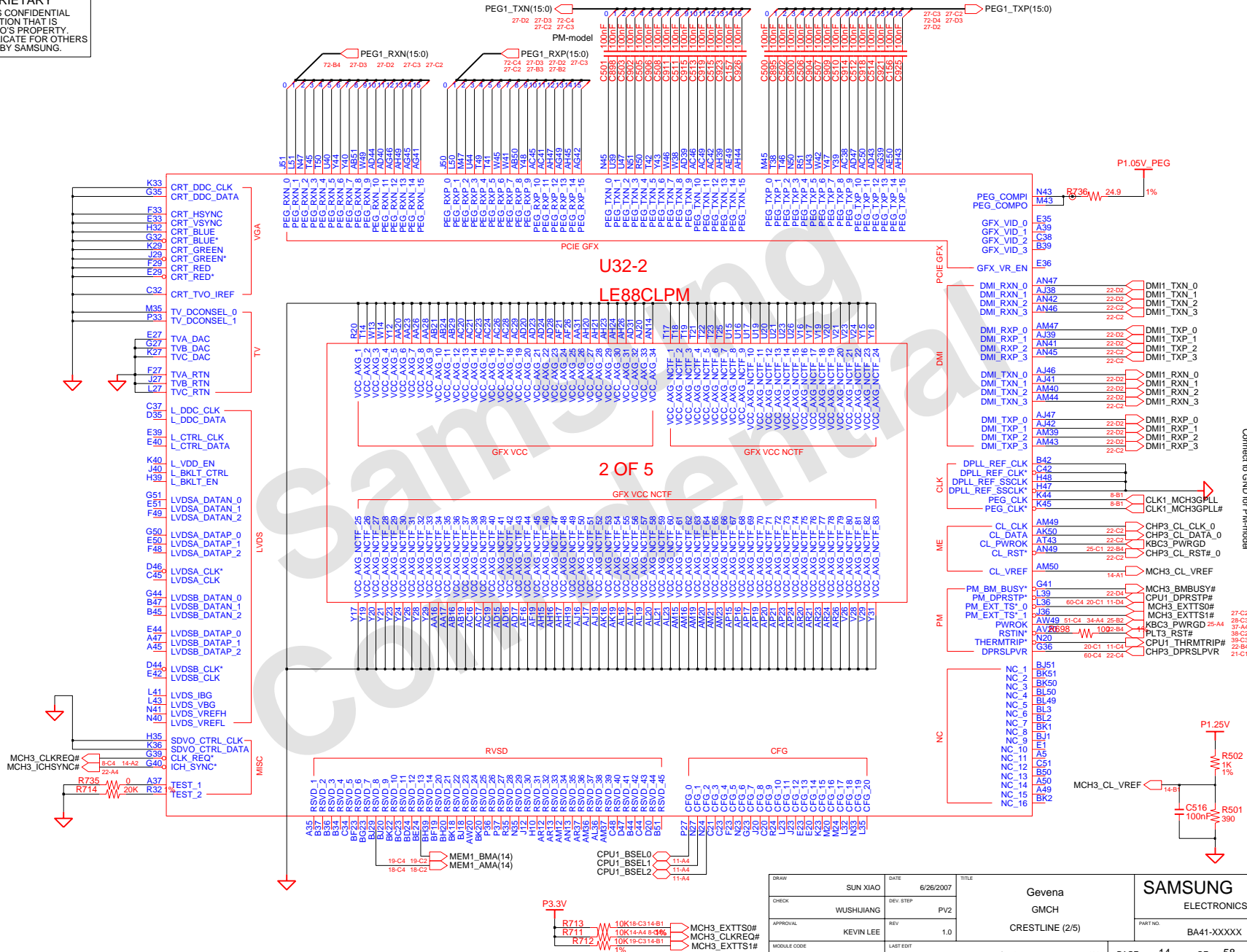
SAMSUNG  
ELECTRONICS  
PART NO.  
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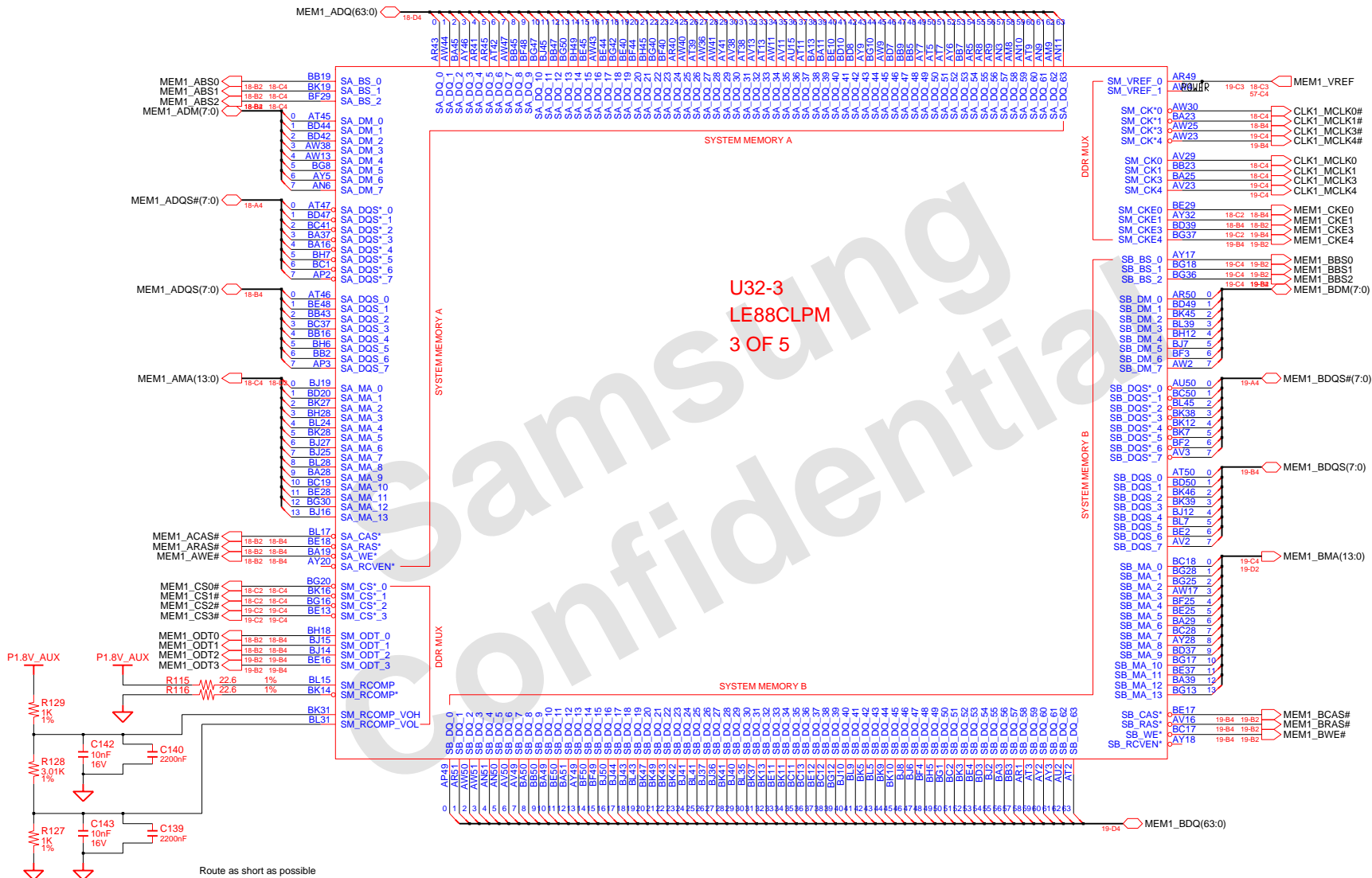


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SUN XIAO		6/26/2007					
CHECK		REV. STEP		<div style="text-align: center;">           Gevena CMCH CRESTLINE (1/5)         </div>		PART NO.	
WUSHUJIANG		PV2				BA41-XXXXX	
APPROVAL		REV					
KEVIN LEE		1.0		CRESTLINE (1/5)			
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM		PAGE 13 OF 58	

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DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2		GMCH	
APPROVAL	KEVIN LEE	REV	1.0		CRESTLINE (3/5)	
MODULE CODE		LAST EDIT				
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[illegible]



[illegible]

*POCAFEb-11 Only (Remove in MP Model)		
Current Setting (def.: default Option)		
CFG#	Low	High
CFG(5)	DmIx2	DmI4x4 (def.)
CFG(6)	Reserved	DDR-I1 (def.)
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(16)	Dynamic ODT Disabled	Dynamic ODT Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	DmI Lane Normal	DmI Lane Revers.
CFG(20)	SDVO or PCIE X1 (def.)	SDVO and PCIE X1 Simultaneously

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Array resistors & Single resistors used to improve layout & routing.

ME POWER RAIL UNDER ME ENABLE

P1.8V\_AUX

DDR1-1  
DDR2-SODIMM-200P-RVS  
1/2

P3.3V

MCH3\_EXTS0#  
MEM1\_VREF

P3.3V

P3.3V

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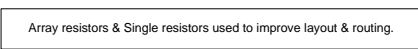
P3.3V

P3.3V

P3.3V

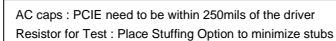
P3.3V

DDR SO-DIMM #1



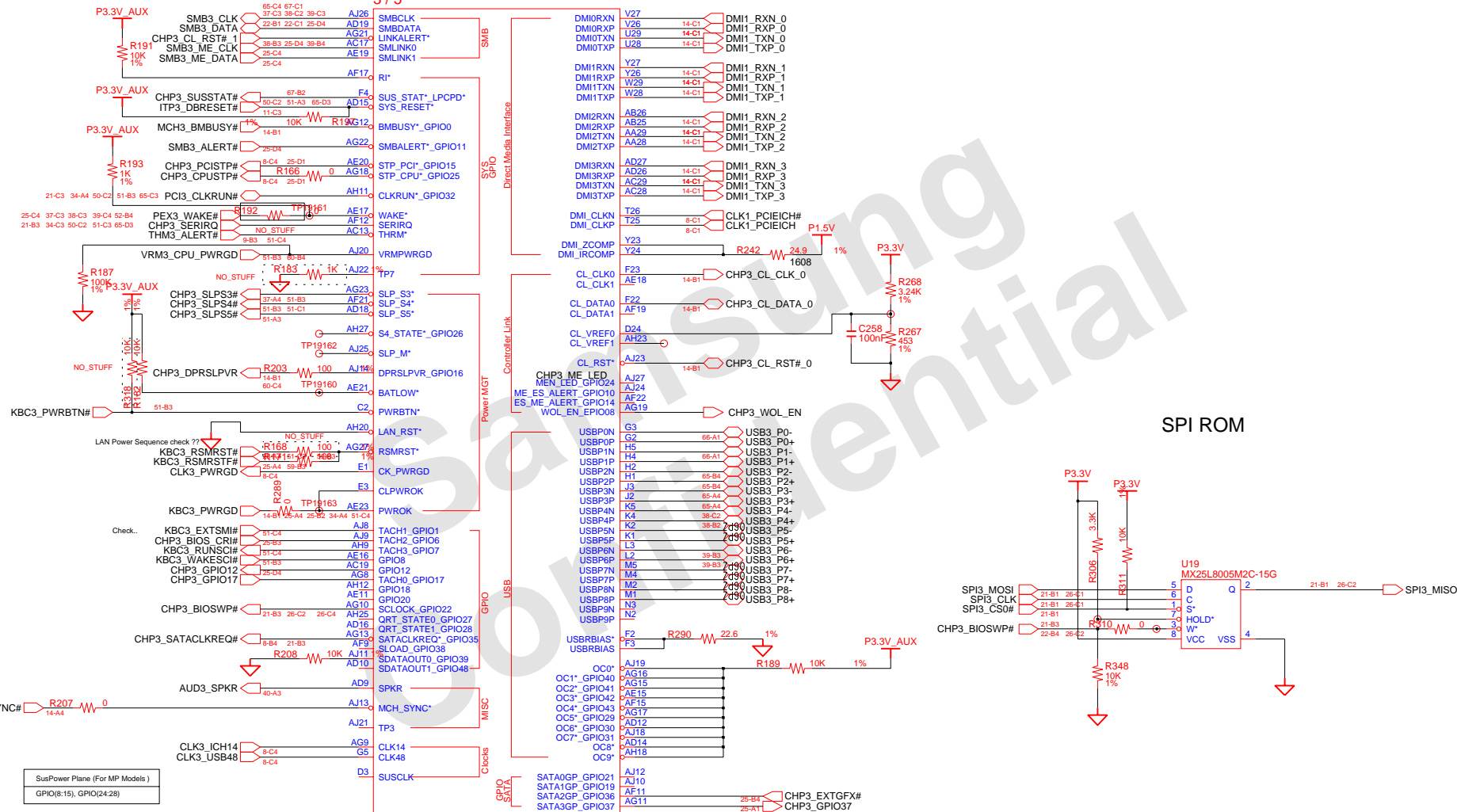
COM-22C-015(1996.6.5) REV. 3

D:/tingting/geneva/Geneva\_pr\_1023

D:/tingting/geneva/Geneva\_pr\_1023

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U33-3  
NH82801HBM  
3 / 5



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena ICH8-M ICH8-M (3/5)	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE	LAST EDIT			October 23, 2007 10:38:02 AM	PAGE	22 OF 58

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**U33-4 NH82801HBM 4/5**

**U33-5 NH82801HBM 5/5**

The schematic diagram illustrates the power distribution network for the U33-4 NH82801HBM 4/5 board. It shows various power planes (VCC1\_5.B, VCC3\_3, VCCCLAN1\_5, etc.) and their connections to components like capacitors, resistors, and diodes. The diagram also includes a detailed view of the U33-5 NH82801HBM 5/5 board, showing its power planes and connections to the U33-4 board. The schematic is labeled with component values, pin numbers, and connector types.

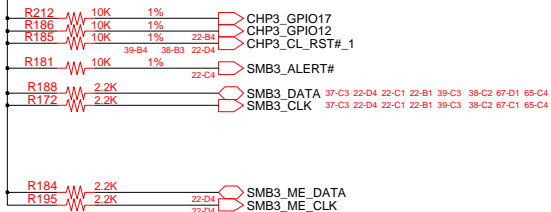
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena
CHECK	WUSHUJIAN	DEV STEP	PV2		ICH8-M
APPROVAL	KEVIN LEE	REV	1.0		ICH8-M (4/5 5/5)
MODULE CODE		LAST EDIT			

October 23, 2007 10:38:02 AM PAGE 23 OF 58

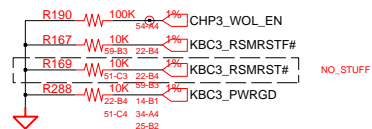
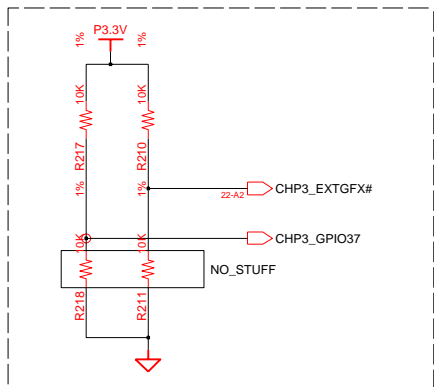


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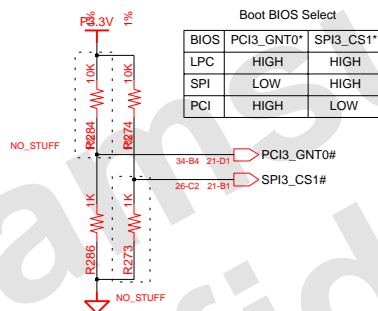
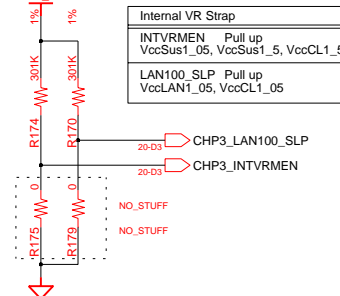
P3.3V\_AUX



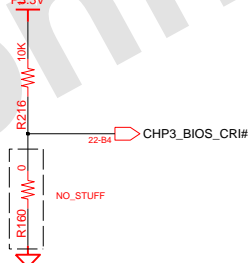
Model Dipendent



PRTC\_BAT



P3.3V



BIOS CRISIS RECOVER STRAP  
PLACE NEAR KEYBOARD

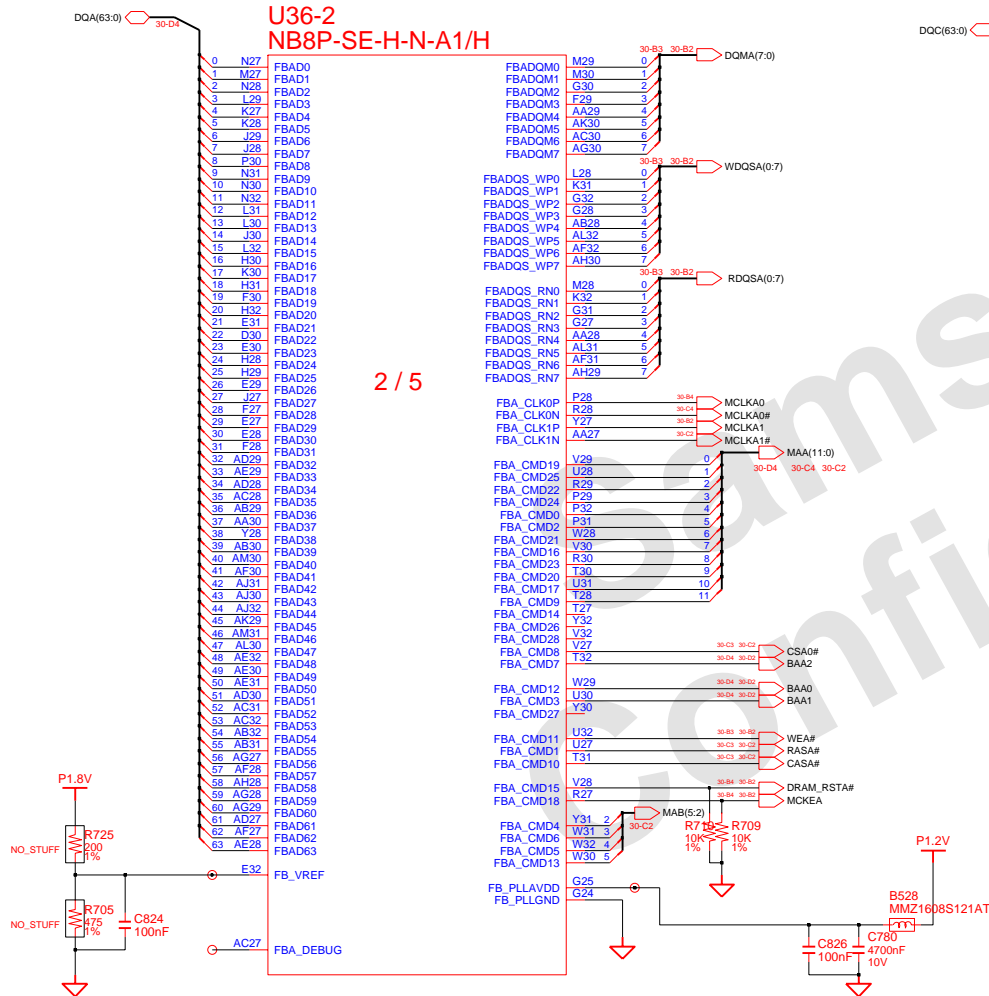
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHUJIANG	DEV. STEP	PV2		ICH8-M	ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0		ICH8-M STAP	PART NO.
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM			BA41-XXXXX
				PAGE	24	OF 58



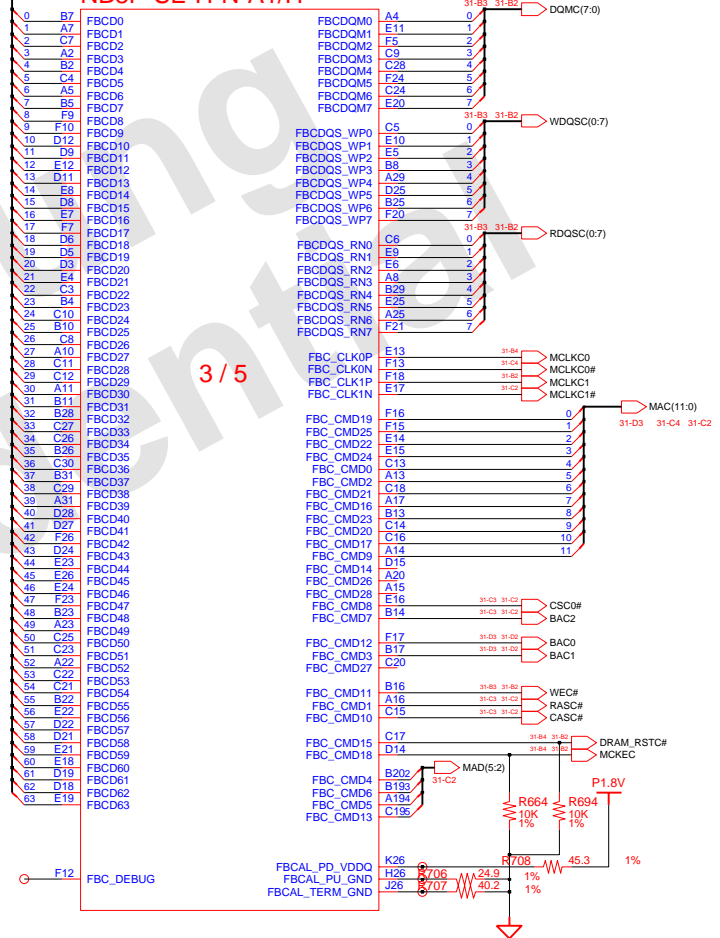
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## Graphic Memory I/F (Using FBA Channel)

## Graphic Memory I/F (Using FBC Channel)



## U36-3 NB8P-SE-H-N-A1/H



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHUJIANG	DEV STEP	PV2		NB8P	ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0		NB8P (2/5 3/5)	PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT				
				October 23, 2007 10:38:02 AM	PAGE 26	OF 58

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**P1.8V**

**EC511**  
330uF  
2.5V  
AL

**C698**  
1000nF  
10V

**C882**  
1000nF  
10V

**C770**  
4700nF  
6.3V

**C880**  
4700nF  
6.3V

**C699**  
100nF  
100nF

**C771**  
100nF

**C831**  
100nF

**C700**  
22nF  
25V

**C820**  
22nF  
25V

**C825**  
22nF  
25V

**C822**  
22nF  
25V

**C821**  
4.7nF  
25V

**C823**  
4.7nF  
25V

**C828**  
4.7nF  
25V

**C829**  
4.7nF  
25V

**C834**  
4.7nF  
25V

**C836**  
4.7nF  
25V

**P1.8V**

**U36-4**  
**NB8P-SE-H-N-A1/H**  
**4 / 5**

**FBVDD\_1**  
GND\_1  
GND\_2  
GND\_3  
GND\_4  
GND\_5  
GND\_6  
GND\_7  
GND\_8  
GND\_9  
GND\_10  
GND\_11  
GND\_12  
GND\_13  
GND\_14  
GND\_15  
GND\_16  
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GND\_29  
GND\_30  
GND\_31  
GND\_32  
GND\_33  
GND\_34  
GND\_35  
GND\_36  
GND\_37  
GND\_38  
GND\_39

**FBVDD\_2**  
GND\_40  
GND\_41  
GND\_42  
GND\_43  
GND\_44  
GND\_45  
GND\_46  
GND\_47  
GND\_48  
GND\_49  
GND\_50  
GND\_51  
GND\_52  
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GND\_57  
GND\_58  
GND\_59  
GND\_60  
GND\_61  
GND\_62  
GND\_63  
GND\_64  
GND\_65

**FBVDD\_3**  
GND\_66  
GND\_67  
GND\_68  
GND\_69  
GND\_70  
GND\_71  
GND\_72  
GND\_73  
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GND\_97  
GND\_98  
GND\_99  
GND\_100

**FBVDD\_4**  
GND\_101  
GND\_102  
GND\_103  
GND\_104  
GND\_105  
GND\_106  
GND\_107  
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GND\_140

**FBVDD\_5**  
GND\_141  
GND\_142  
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**FBVDD\_6**  
GND\_201  
GND\_202  
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GND\_300

**FBVDD\_7**  
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GND\_302  
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GND\_400

**FBVDD\_8**  
GND\_401  
GND\_402  
GND\_403  
GND\_404  
GND\_405  
GND\_406  
GND\_407  
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GND\_437  
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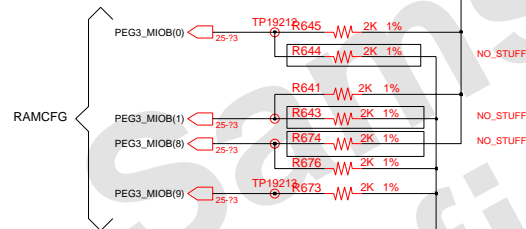
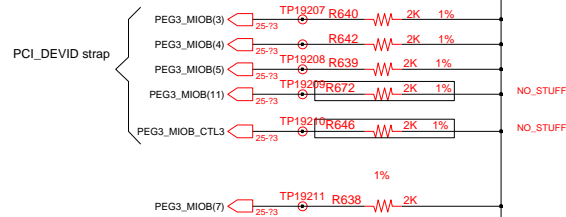
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DRAW		DATE		<div> <div>6/26/2007</div> <div> <div>Gevena</div> <div>NB8P</div> <div>NB8P (5/5)</div> </div> </div>		<div> <div>SAMSUNG</div> <div>ELECTRONICS</div> <div>PART NO.</div> <div>BA41-XXXXX</div> </div>	
SUN XIAO		6/26/2007					
CHECK		DEV. STEP					
WUSHUJIANG		PV2					
APPROVAL		REV		1.0			
KEVIN LEE							
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM		PAGE	28 OF 58

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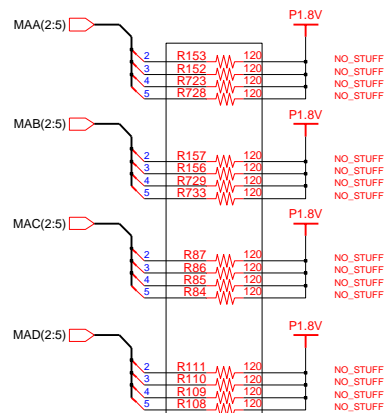
PCI\_DEVID strap

	R646	R672	R640	R639	R642
NB8P-SE	NO_STUFF	NO_STUFF	STUFF	NO_STUFF	STUFF
NB8M-GS	0	0	1	1	1
	NO_STUFF	NO_STUFF	STUFF	STUFF	STUFF
	0	0	1	1	1



RAMCFG

	R674	R676	R641	R643
SS 256Mbit	STUFF	NO_STUFF	STUFF	NO_STUFF
IF 256Mbit	STUFF	NO_STUFF	NO_STUFF	STUFF
SS 512Mbit	NO_STUFF	STUFF	STUFF	NO_STUFF
IF 512Mbit	NO_STUFF	STUFF	NO_STUFF	STUFF



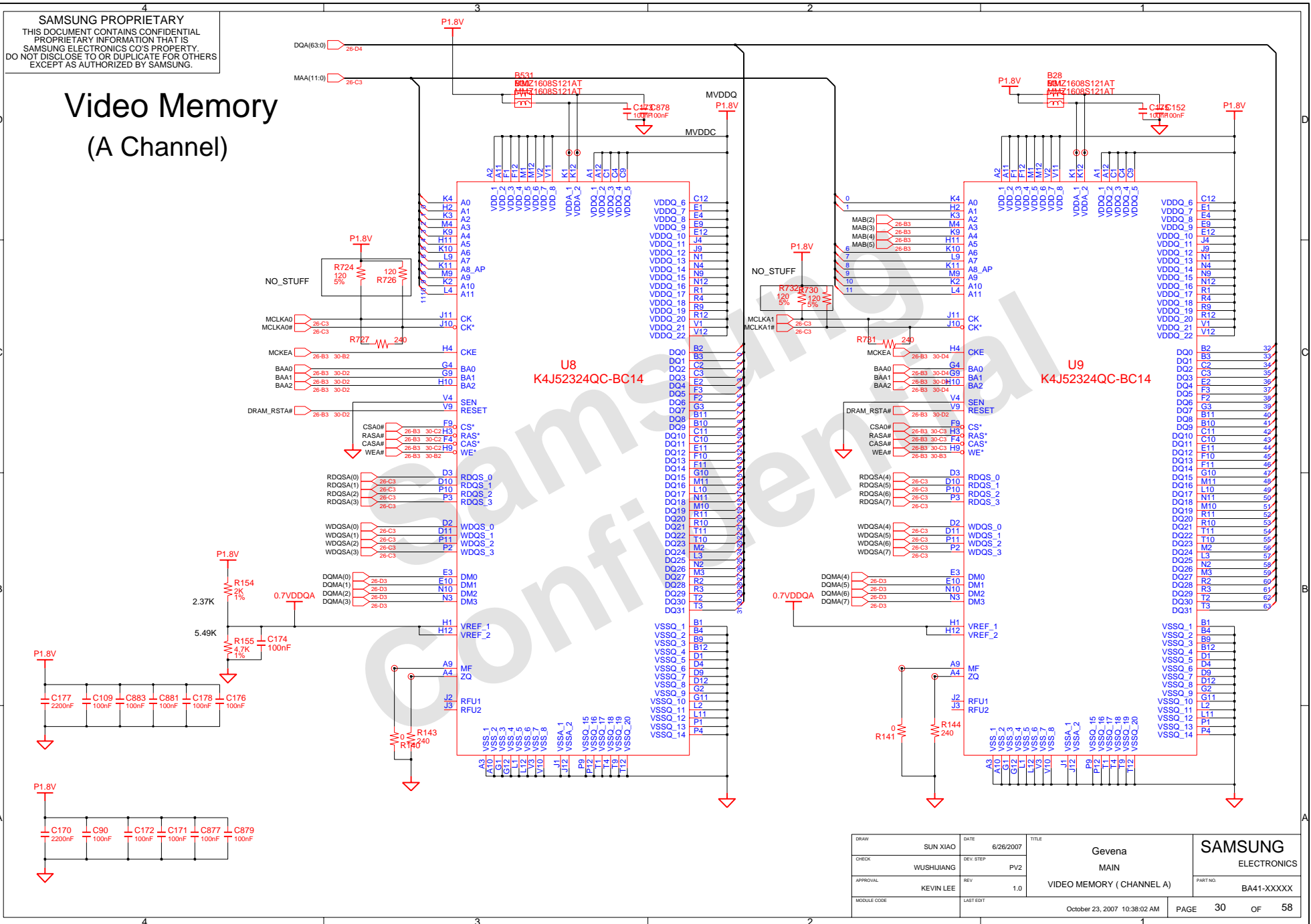
Straps	Pin # (Rev.A02)	Descriptions
SUB_VENDOR	MIOAD(1)	0 : No BIOS 1 : Read from BIOS
RAMCFG(3:0) [9,8,1,0]	MIOB(9) MIOB(8) MIOB(1) MIOB(0)	0111 : SAMSUNG GDDR3 256Mbit 0101 : INFINEON GDDR3 256Mbit 0011 : SAMSUNG GDDR3 512Mbit 0001 : INFINEON GDDR3 512Mbit
CRYSTAL(1:0)	MIOB(2) MIOB(6)	01 : 14.318 MHz 10 : 27 MHz 11 : Unknown 00 : 13.5 MHz
TV_MODE(1:0)	MIOAD(7) MIOAD(10)	00 : SECAM 01 : NTSC 10 : PAL 11 : CRT
PCI_DEVID(4:0) [CTL3,11,3,5,4]	MIOB_CTL(3) MIOB(11) MIOB(3) MIOB(5) MIOB(4)	NB8M-GS: 00111 NB8M-SE: 01000 NB8M-GT: 00110 NB8P-GS: 00111 NB8P-SE: 00101 NB8P-GT: 01000
ROM_TYPE(1:0)	MIOB(10) MIOBVSYN	NO ROM(NC)
USER STRAP	MIOAD(2:5)	EDID
GPIO(12:0)	Sheet 25	Refer to Sheet 25

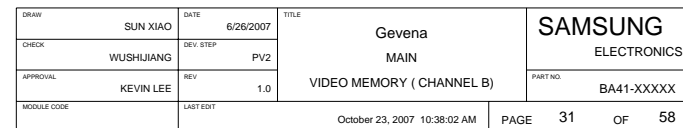
Test Options for GPIO should be updated..

Samsung		Infineon	
256Mbit	512Mbit	256Mbit	512Mbit
K4J55323QG (1.2/1.4/1.6/2.0) K4J55323QF (1.4/1.6/2.0)	K4J52324QC (1.2/1.4/1.6/2.0)	HYB18H256321AF-20(2.0) HYB18H256321AF-16(1.6) HYB18H256324AF-20(2.0) HYB18H256321AF-14(1.4) HYB18H256321AF-12(1.2)	HYB18H512321AF-20(2.0) HYB18H512321AF-16(1.6) HYB18H512324AF-20(1.6) HYB18H512321AF-14(1.4) HYB18H512321AF-12(1.2)
8M*32BIT	16M*32BIT	8M*32BIT	16M*32BIT

DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS PART NO. BA41-XXXXX
CHECK	WUSHUJIANG	DEV. STEP	PV2		NB8P	
APPROVAL	KEVIN LEE	REV	1.0		NB8P STRAP	
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM		
					PAGE	29 OF 58

# Video Memory (A Channel)

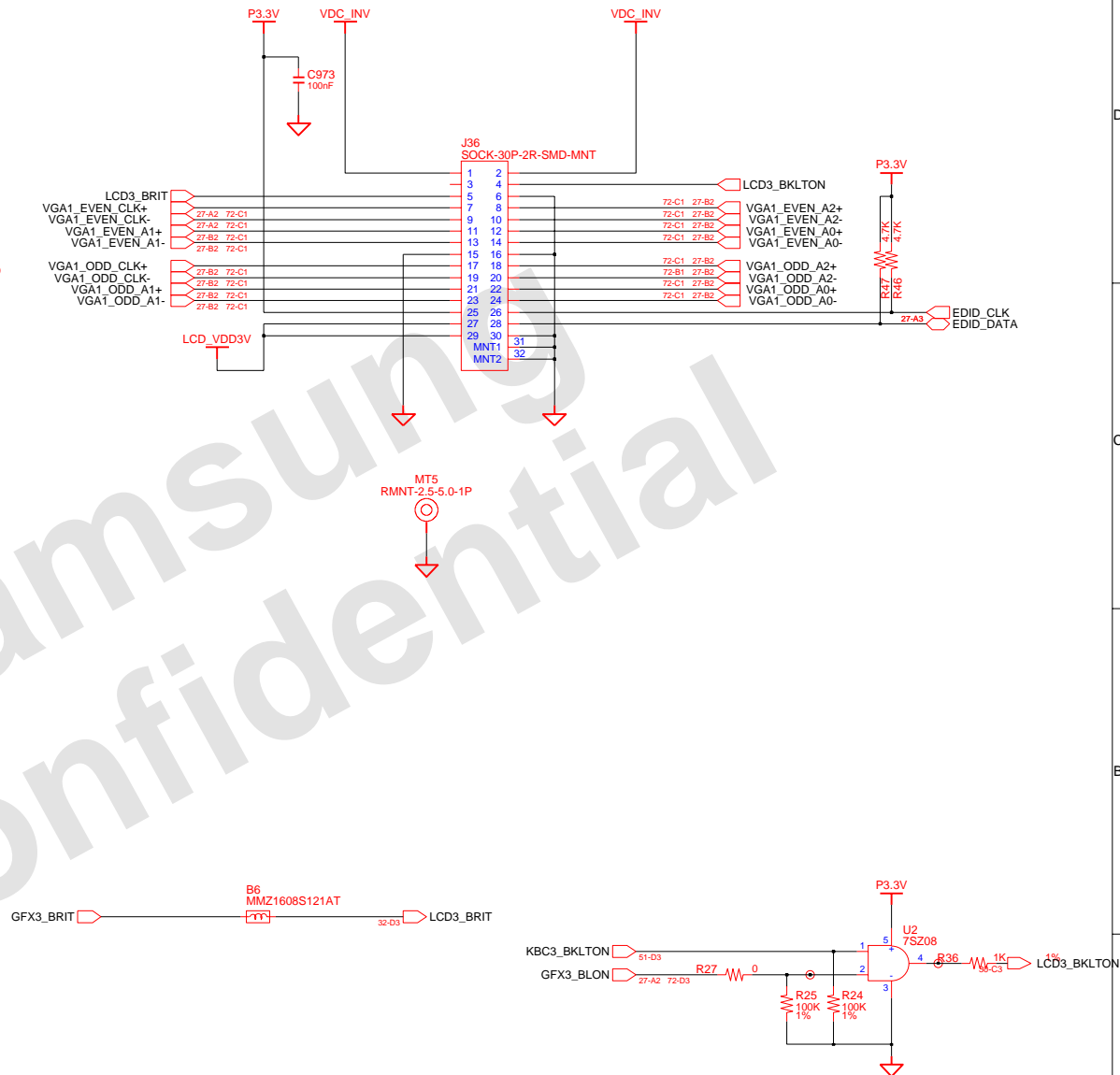
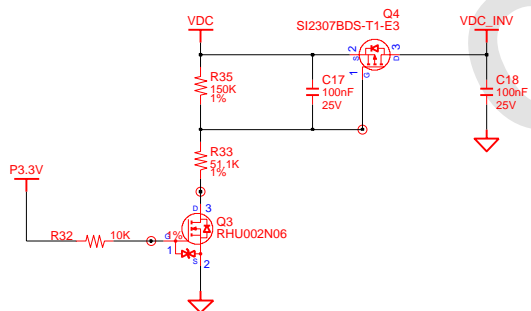
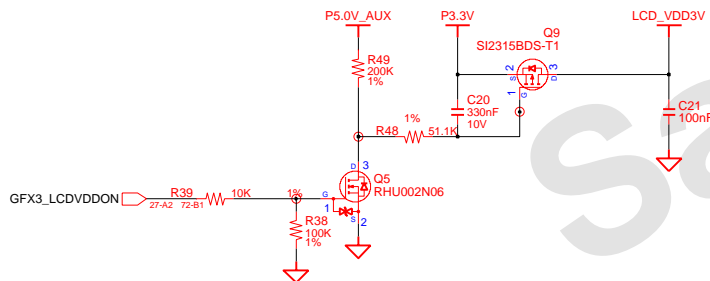
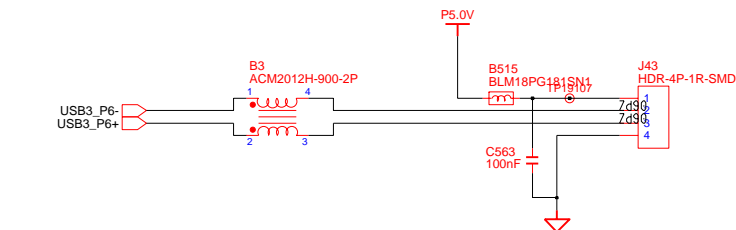






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## USB CAMERA FUNCTION

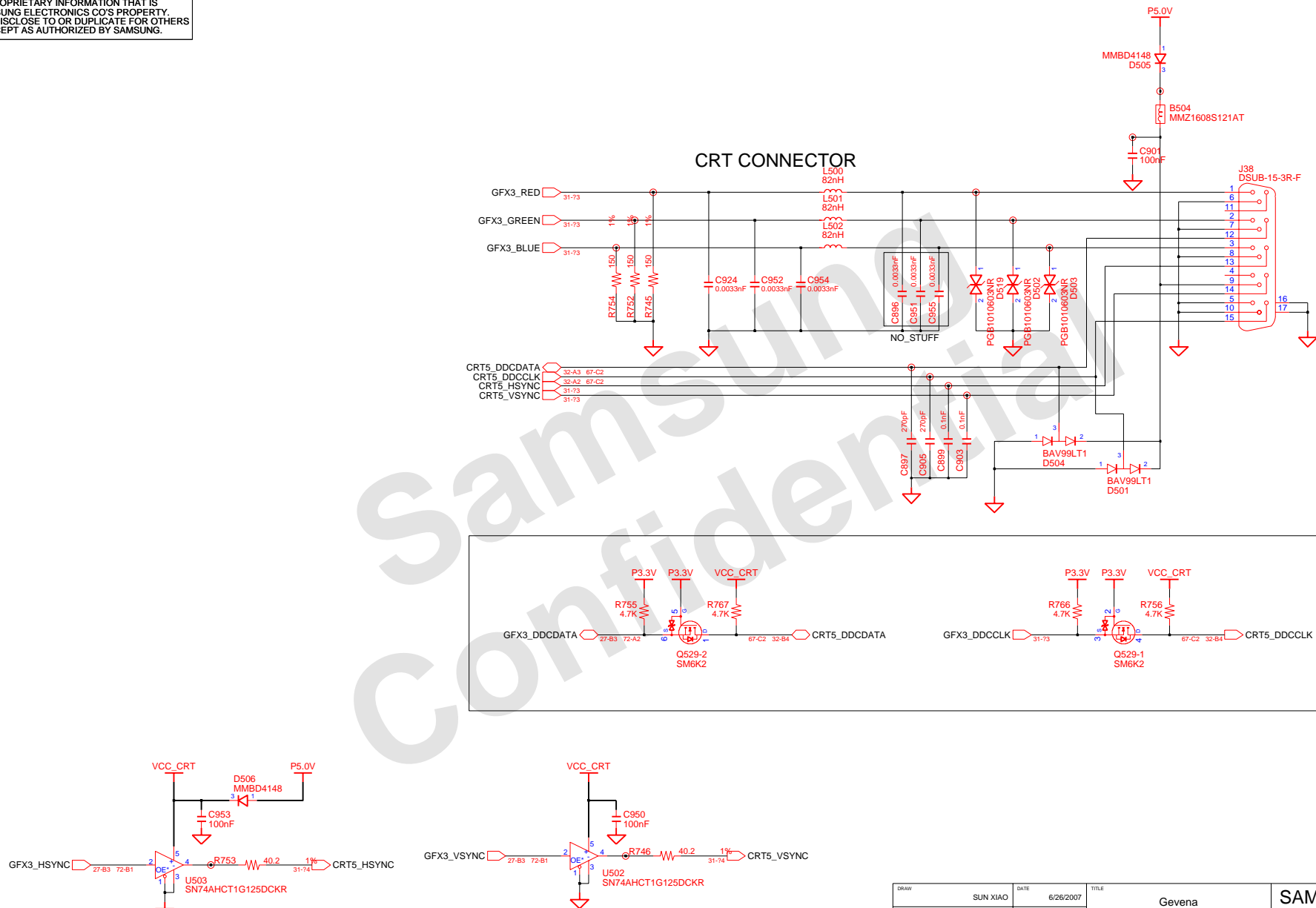


DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHUIJIANG	DEV. STEP	PV2	LCD CONNECTER & SPEED SPECTRUM		ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0		PART NO.	BA41-XXXXX
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	32	OF 58



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## CRT CONNECTOR



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena MIAN CRT PORT	SAMSUNG ELECTRONICS PART NO. BA41-XXXXX
CHECK	WUSHUIJANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT				
October 23, 2007 10:38:02 AM						PAGE 33 OF 58

4

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C

B

A

COM-22C-015(1996.6.5) REV. 3

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Option

U516  
LPC47N207

P3.3V P3.3V

VCC1  
VCC2  
VCC3  
VCC4  
VCC5

VTR

GPIO10  
GPIO11  
GPIO12\_IO\_SMI\*  
GPIO13\_IRQIN1  
GPIO14\_IRQIN2  
GPIO15  
GPIO16  
GPIO17  
GPIO30  
GPIO31  
GPIO32  
GPIO33  
GPIO34  
GPIO35  
GPIO36  
GPIO37

IRTX2  
IRRX2  
IRMODEM\_IPRX3

VSS1  
VSS2  
VSS3  
VSS4  
VSS5  
VSS6

GND

KBC3\_PWRGD

R662

TP19216

P3.3V

R663  
10K 1%

LPC3\_LAD(3:0)

LAD\_0  
LAD\_1  
LAD\_2  
LAD\_3

\*LFRAME  
\*LDRQ0  
\*LDRQ1  
\*PCI\_RESET  
\*LPCPD  
\*CLKRUN  
SER\_IRQ  
\*IO\_PME  
PCI\_CLK  
LPC\_CLK\_33  
SIO\_14M

LPC3\_LFRAME#  
CHP3\_LDRQ0#  
CHP3\_LDRQ1#  
PLT3\_RST#  
CHP3\_SUSSTAT#  
PCI3\_CLKRUN#  
CHP3\_SERIRQ

TP19218

CLK3\_PCLKSIO  
CLK3\_PCLKSIO\_DS  
CLK3\_SIO14

DLAD\_0  
DLAD\_1  
DLAD\_2  
DLAD\_3

\*DLFRAME  
\*DLDRQ1  
\*DCLKRUN  
DSER\_IRQ  
DLPC\_CLK\_33  
DSIO\_14M

RX01  
TXD1  
\*DSR1  
\*CTS1  
\*RT1  
\*DCD1  
RTS1\*\_SYSOTPO  
DTR1\*\_SYSOTPO

SIO3\_RXD1  
SIO3\_TXD1  
SIO3\_DSR1#  
SIO3\_CTS1#  
SIO3\_RI1#  
SIO3\_DCD1#  
SIO3\_RTS1#  
SIO3\_DTR1#

R617 10K 1%  
R618 10K 1%

P3.3V

P5.0V

J40  
HDR-10P-SMD

SIO3\_DTR1#  
SIO3\_TXD1  
SIO3\_RTS1#  
SIO3\_CTS1#  
SIO3\_RI1#  
SIO3\_RXD1  
SIO3\_DSR1#  
SIO3\_DCD1#

MNT1  
MNT2

Option

DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena SIO CHIPSET
CHECK	WUSHUJIANG	DEV STEP	PV2		
APPROVAL	KEVIN LEE	REV	1.0		
MODULE CODE		LAST EDIT			

October 23, 2007 10:38:02 AM

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SAMSUNG  
ELECTRONICS

PART NO.  
BA41-

Option

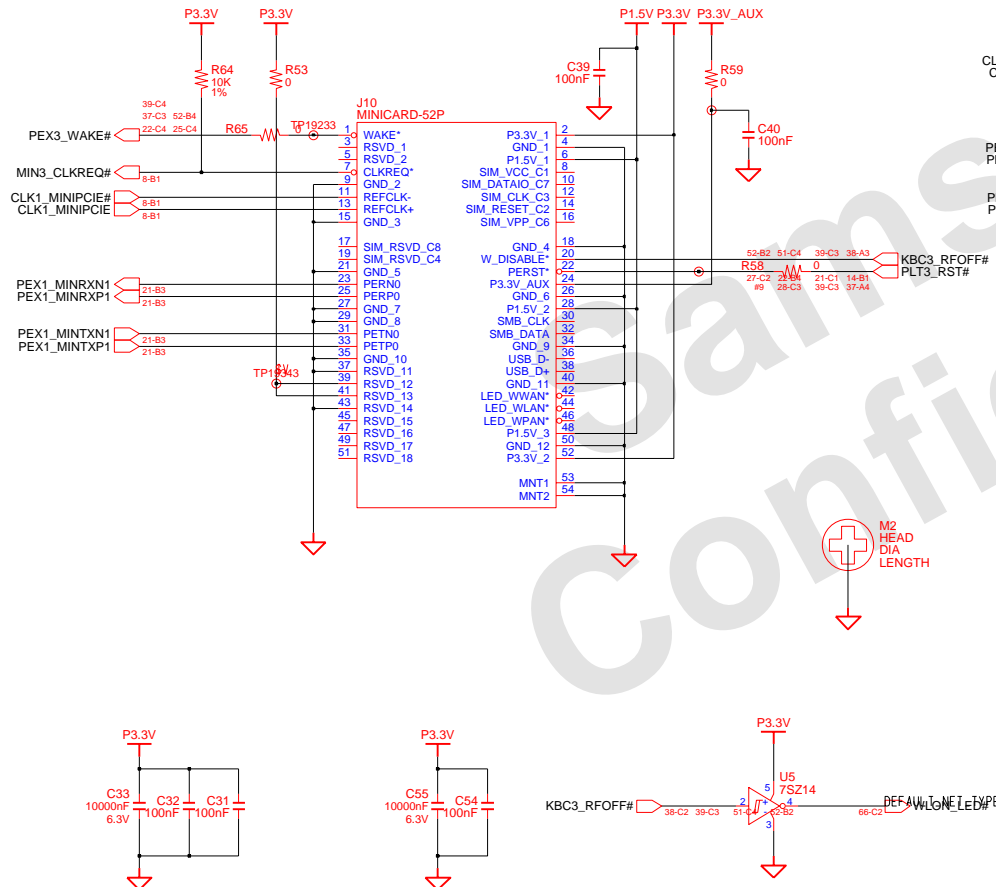
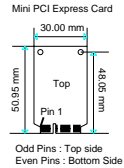
DRAW		DATE	TITLE		<div>SAMSUNG ELECTRONICS</div>		
SUN XIAO		6/26/2007	<div>Gevena SIO CHIPSET</div>				
CHECK	WUSHUJIANG	DEV. STEP					PV2
APPROVAL	KEVIN LEE	REV					1.0
				PART NO.		BA41-	
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM		PAGE 34 OF 68	

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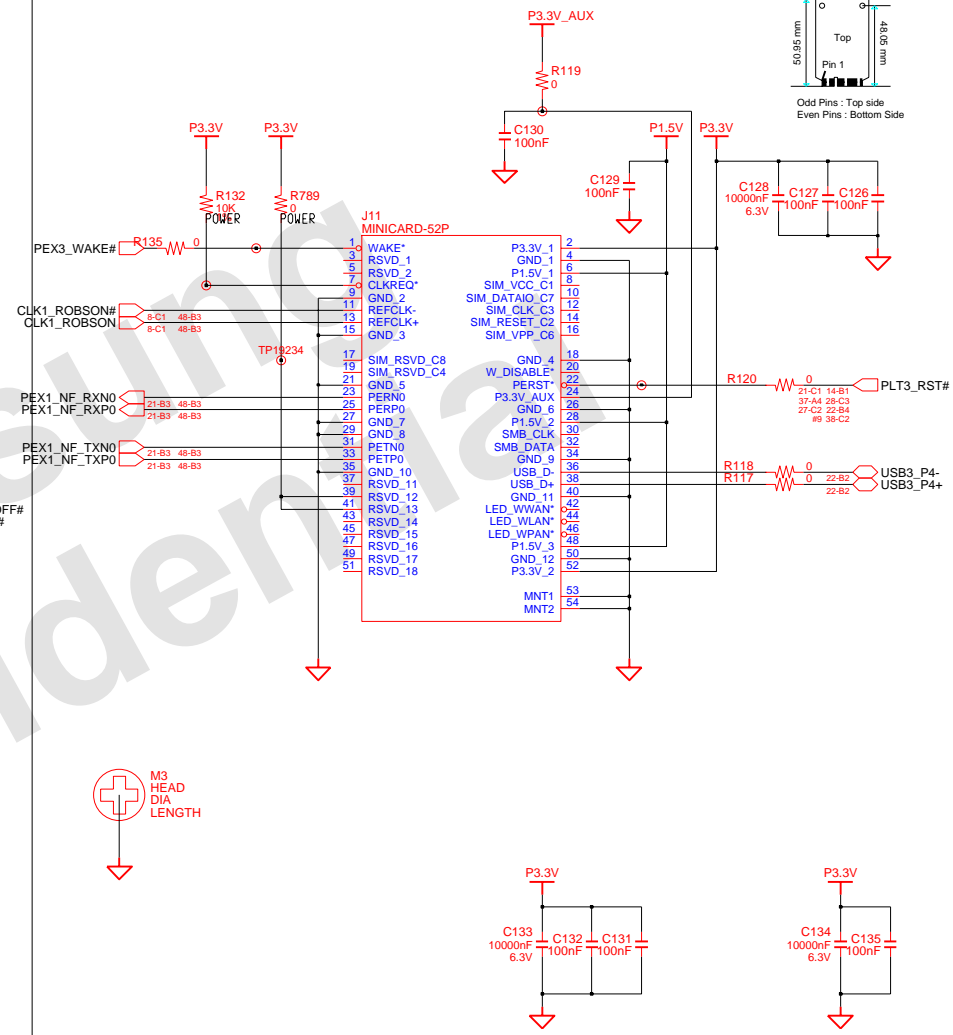
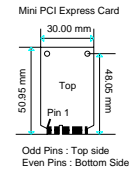
D:/tingting/geneva/Geneva\_pr\_102

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## Mini Card

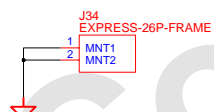
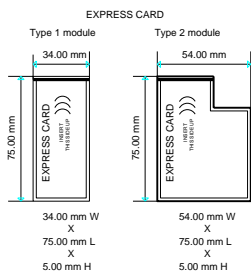


## MINI CARD FOR ROBSON



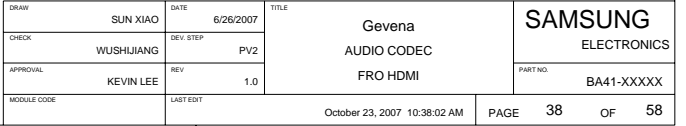
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CHECK	WUSHUJIANG	DEV. STEP	PV2		MINI CARD	ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0		FRO BOBSON AND DVB-T	PART NO.
MODULE CODE		LAST EDIT				BA41-XXXXX
				October 23, 2007 10:38:02 AM	PAGE	36 OF 58

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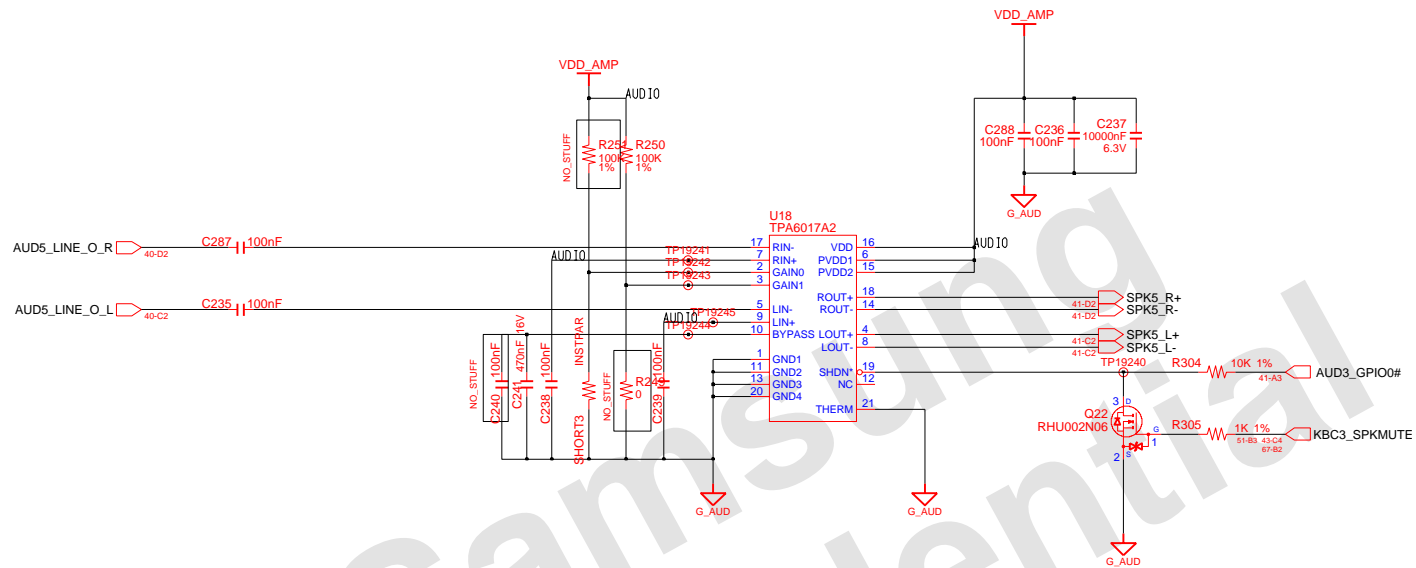


DRUM	SUN XIAO	DATE	6/27/2007	TITLE  Geneva MIO BOARD EXPRESS CARD	SAMSUNG ELECTRONICS
CHECK	WUSHIJIANG	DEV. STEP	PV2		
APPROVAL	KEVIN LEE	REV	1.0		
MODULE CODE	LAST EDIT		October 23, 2007 10:38:02 AM		
				PART NO.	BA41-XXXX

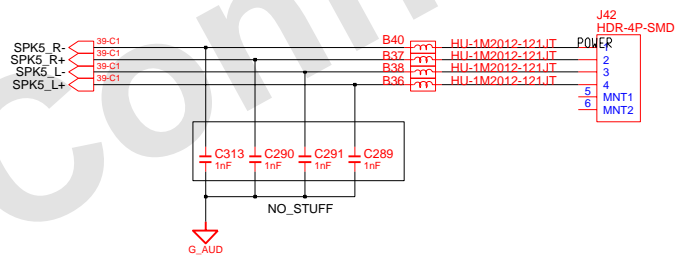
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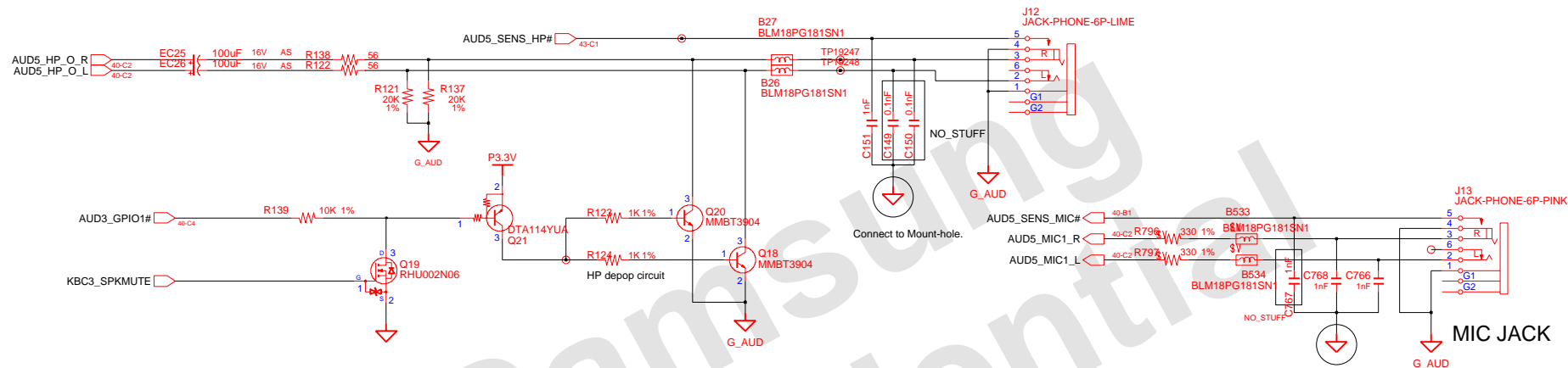
### INTERNAL STEREO SPEAKERS



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena AUDIO AMP	SAMSUNG ELECTRONICS
CHECK	WUSHUIJANG	DEV. STEP	PV2			PART NO. BA41-XXXXX
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	39	OF 58

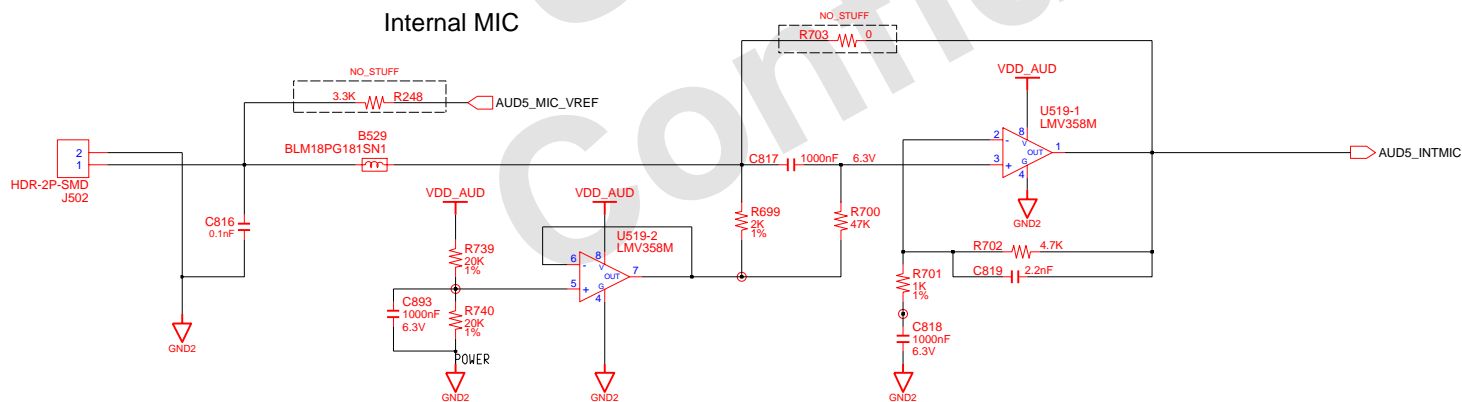
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## HEADPHONE



The traces led to Audio Jacks have the width over 10mil

## Internal MIC

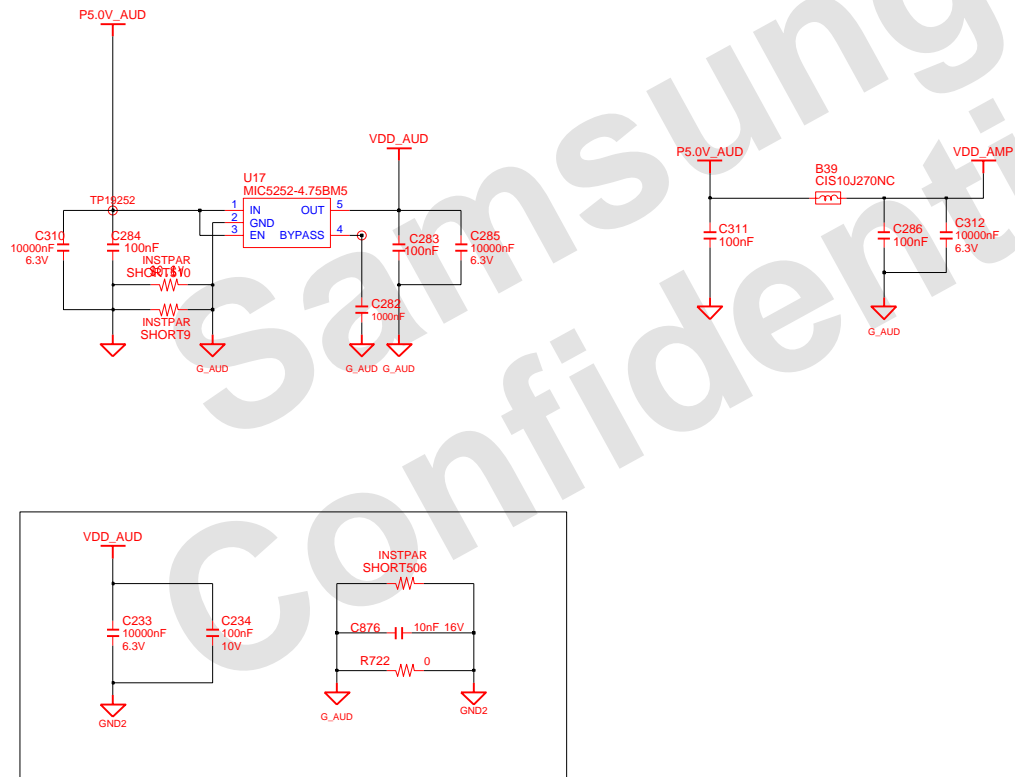


DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2		HEAD PHONE JACK	
APPROVAL	KEVIN LEE	REV	1.0		AND MIC JACK	
MODULE CODE		LAST EDIT				
October 23, 2007 10:38:02 AM						PAGE 40 OF 58



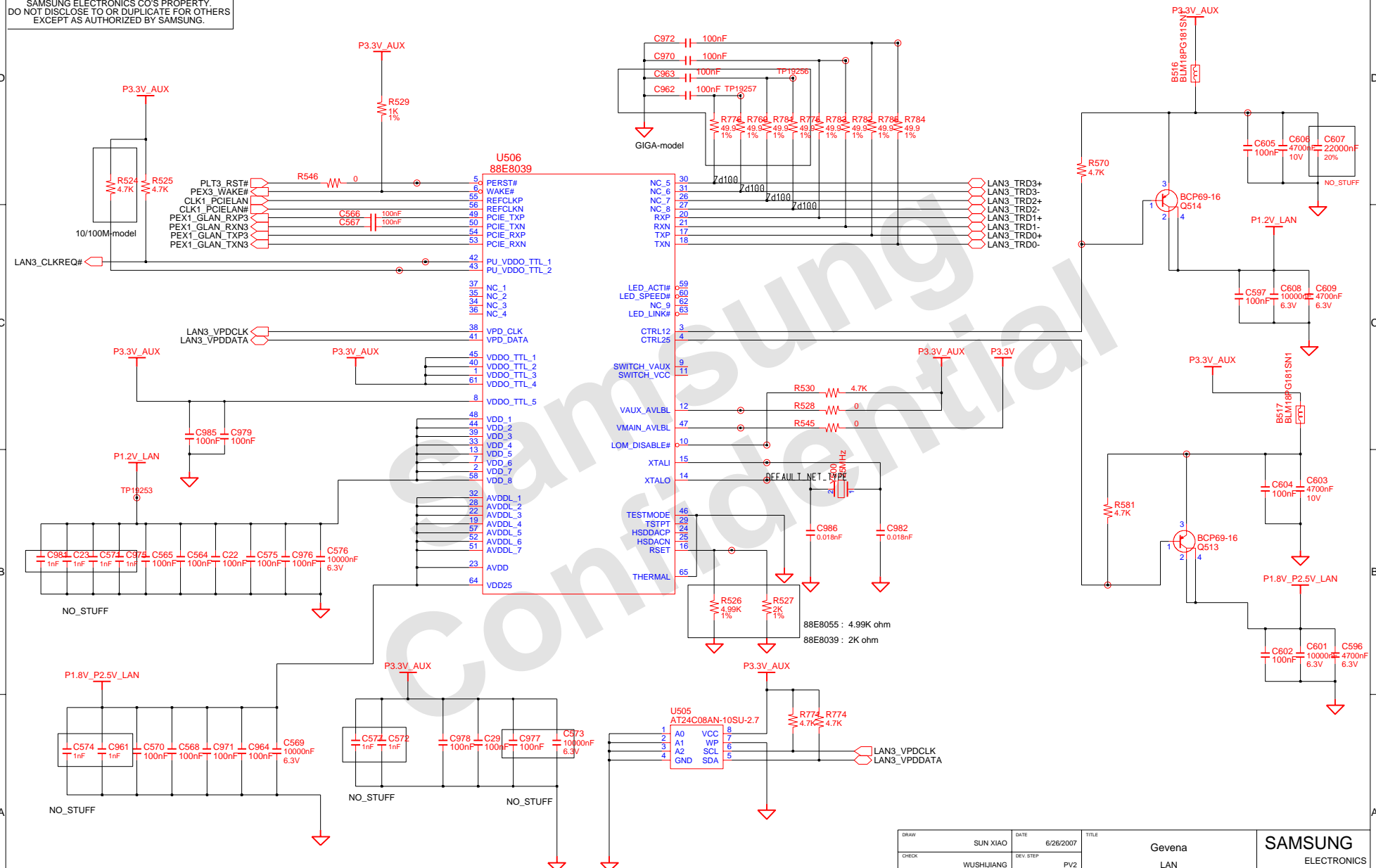
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# AUDIO POWER



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena AUDIO AUDIO POWER	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2			PART NO. BA41-XXXXX
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	41	OF 58

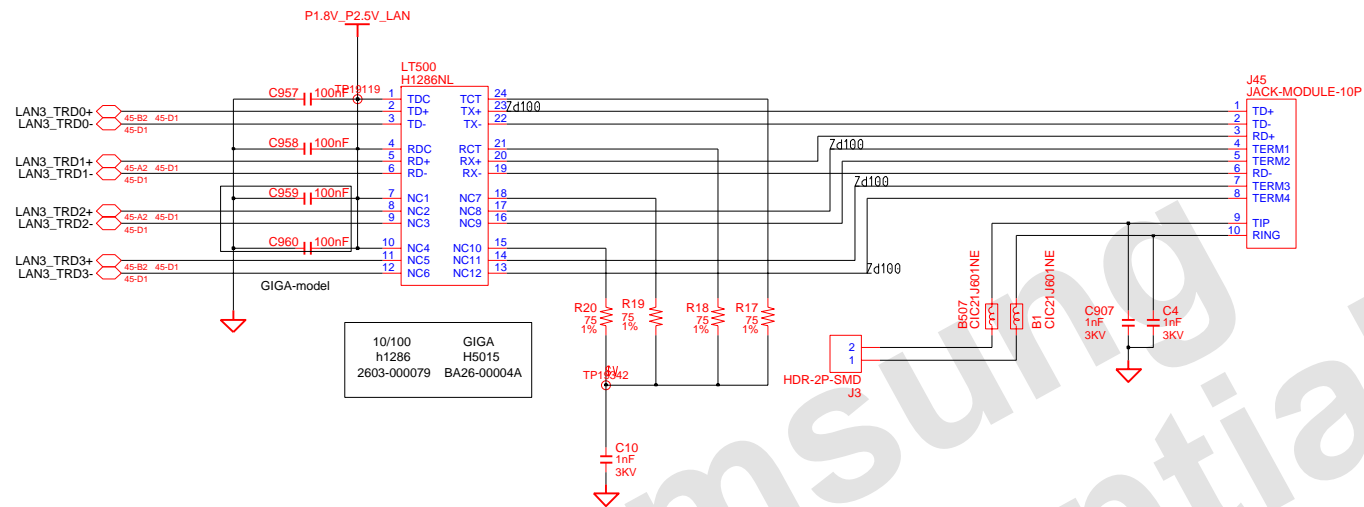
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DRAW	SUN XIAO	DATE	6/26/2007	<div>Gevena LAN 88E8055</div> <div>SAMSUNG ELECTRONICS</div>			
CHECK	WUSHUJIANG	DEV STEP	PV2				
APPROVAL	KEVIN LEE	REV	1.0			<div>PART NO.</div> <div>BA41-XXXXX</div>	
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	42	OF 58

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The distance between LAN controller  
and transformer is designed to extend less than two inches.

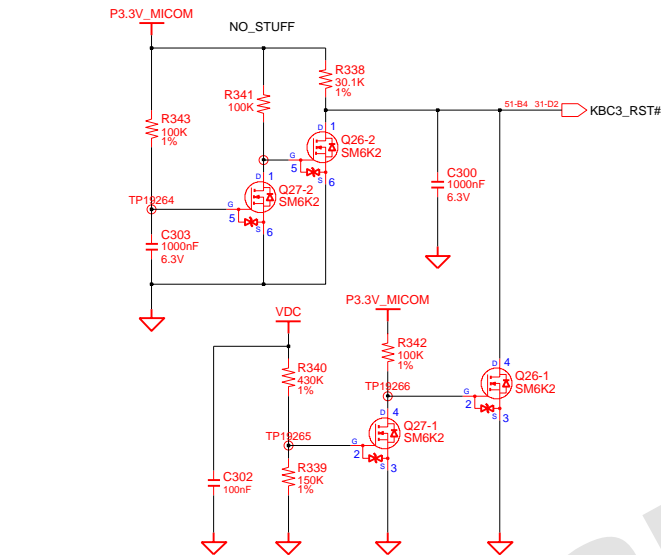


DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHUIJANG	DEV. STEP	PV2	LAN	LAN JACK RJ45	ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0			PART NO.
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM			BA41-XXXXX
				PAGE	43	OF 58

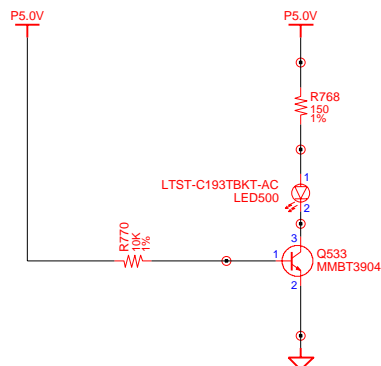
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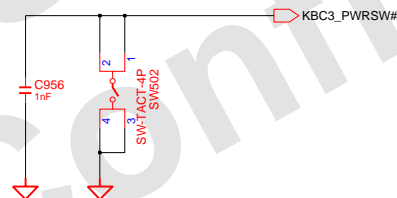
## MICOM RESET



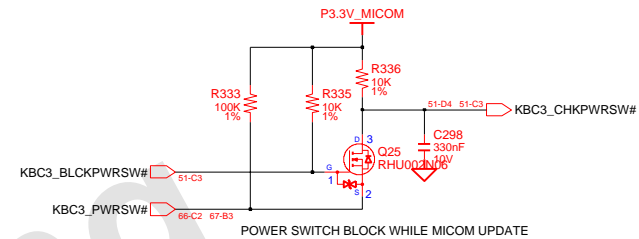
## POWER ON LED



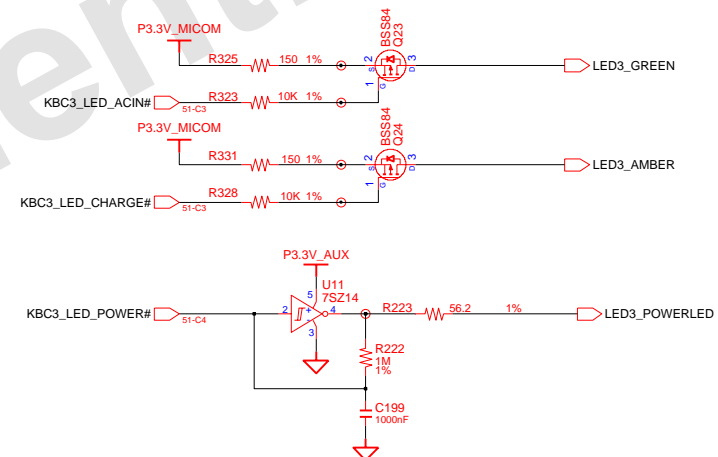
## POWER ON SW BUTTON



## FOR MICOM UPDATE



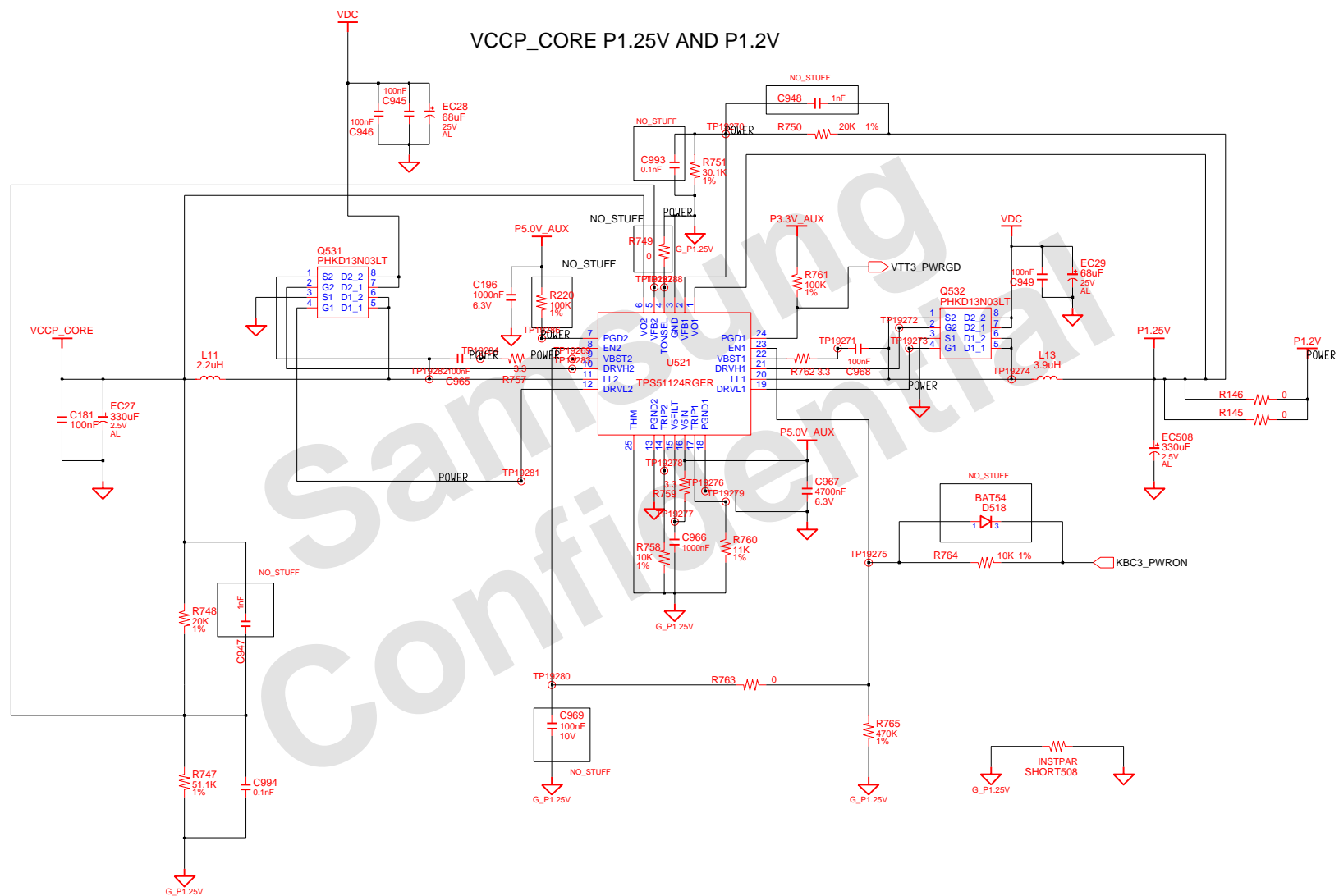
## ADAPTERIN/CHARGING LED



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUIJANG	DEV. STEP	PV2		MICOM	
APPROVAL	KEVIN LEE	REV	1.0		MICOM LOGIC SCH	
MODULE CODE		LAST EDIT				
October 23, 2007 10:38:02 AM						PAGE 45 OF 58

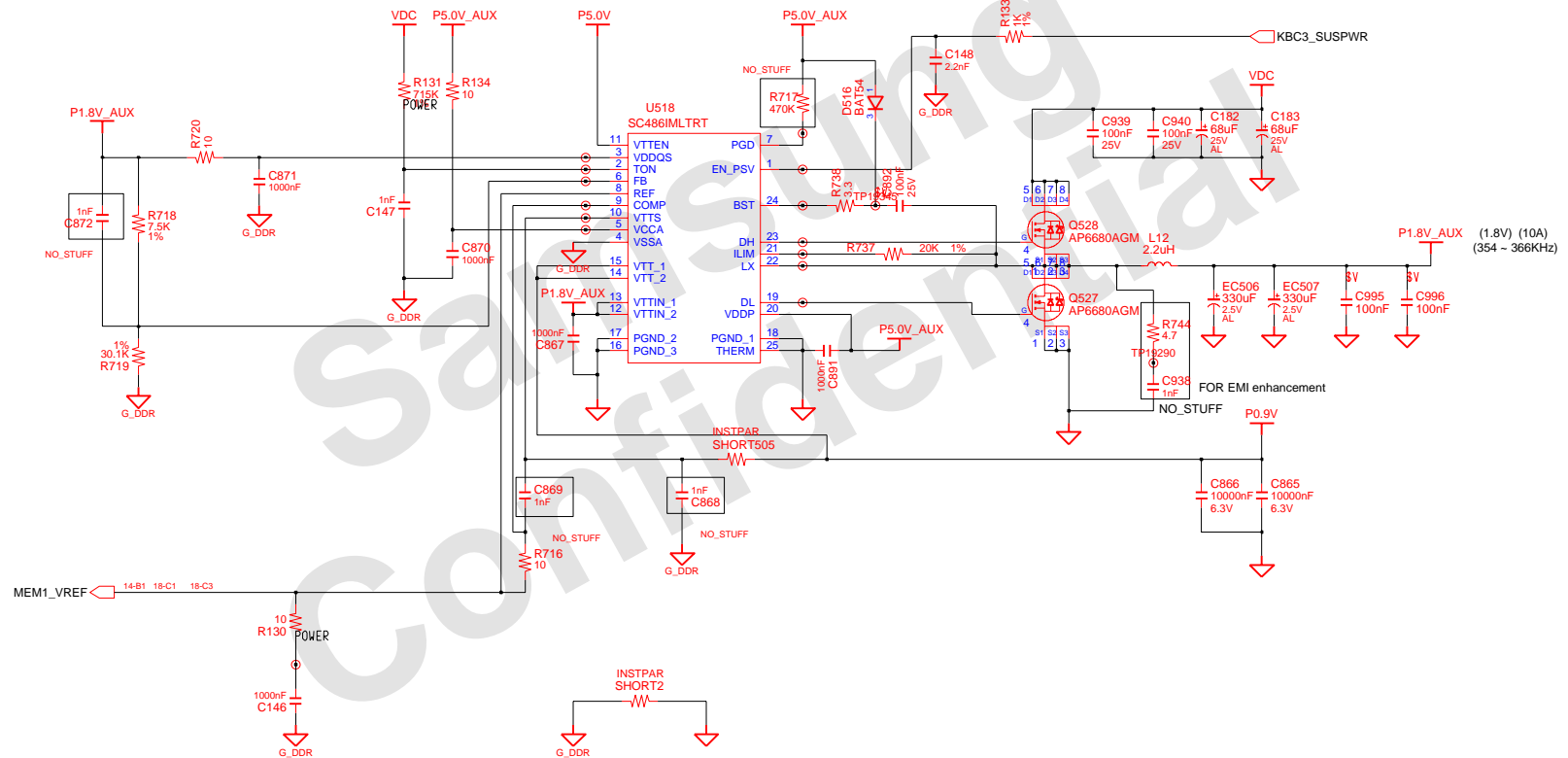


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DRAWN	SUN XIAO	DATE	6/26/2007	Gevena MAIN VCCP P1.25V AND P1.2V		SAMSUNG ELECTRONICS		
CHECK	WUSHUJIANG	DEV. STEP	PV2					
APPROVAL	KEVIN LEE	REV	1.0			PART NO.	BA41-XXXXX	
MODULE CODE	LAST EDIT			October 23, 2007 10:38:02 AM	PAGE	47	OF	58

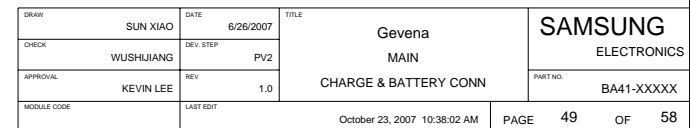
## DDR2 Power



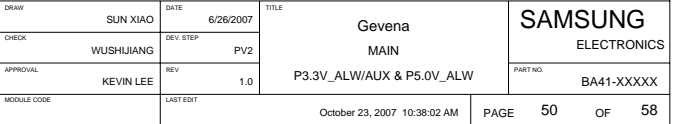
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena MAIN DDR2 POWER	SAMSUNG ELECTRONICS
CHECK	WUSHUIJANG	DEV. STEP	PV2			PART NO. BA41-XXXXX
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT				
				October 23, 2007 10:38:02 AM	PAGE 48 OF 58	



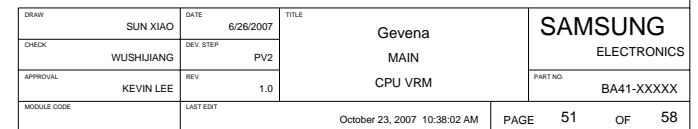
## CHARGER & POWER MANAGEMENT



## P3.3V\_ALW/AUX & P5V\_AUX

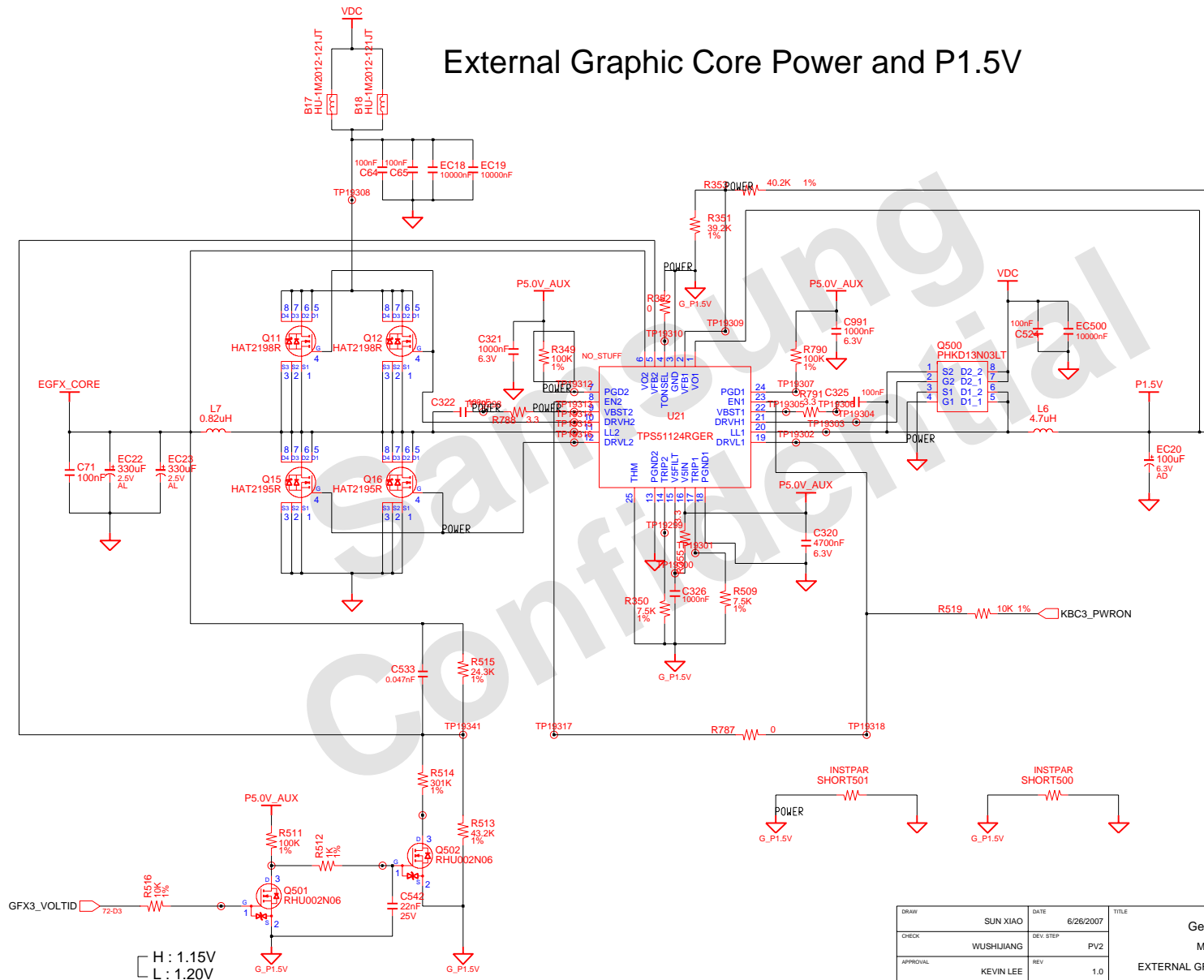


CPU VRM [SEMTECH]

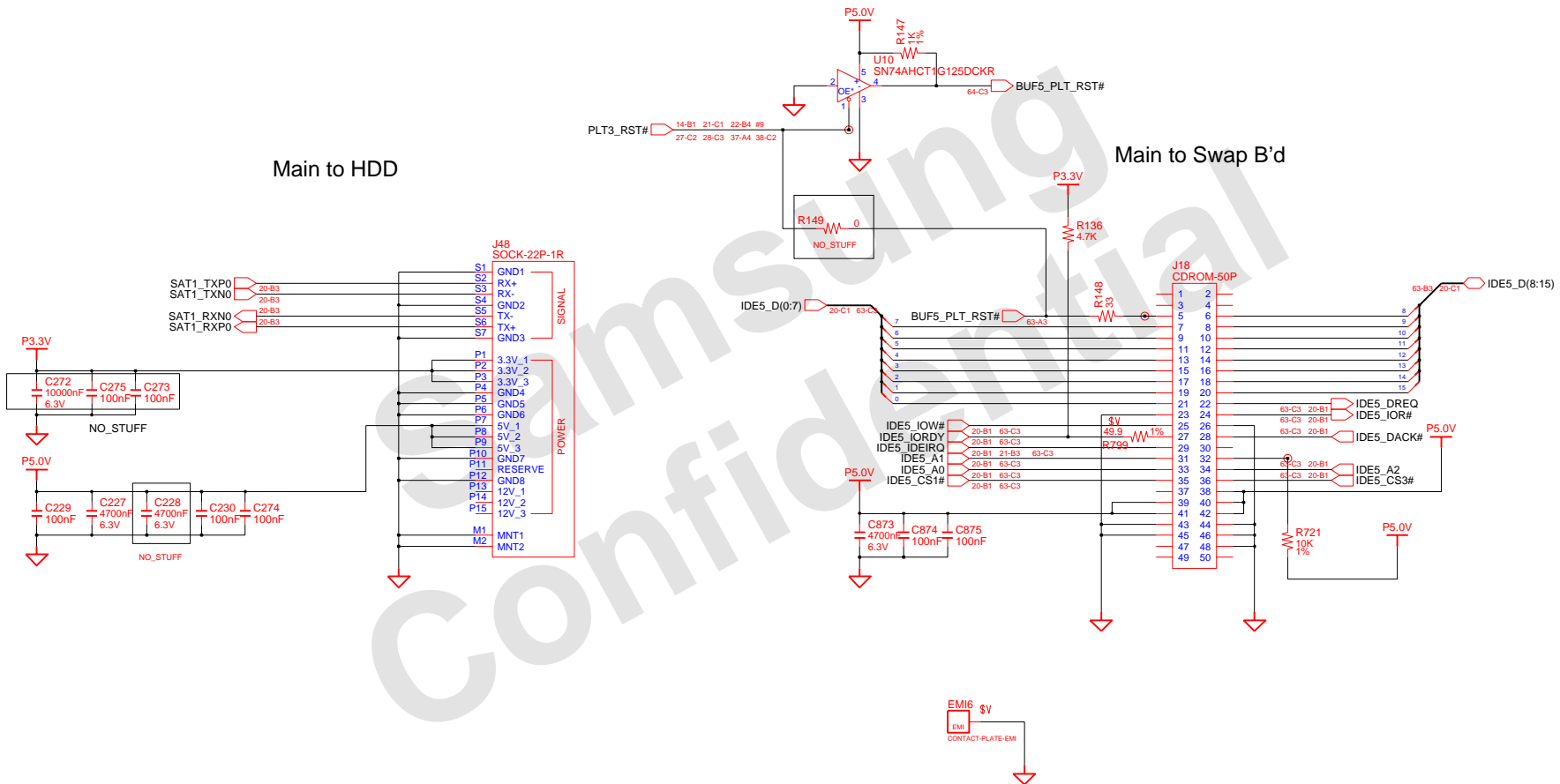


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## External Graphic Core Power and P1.5V



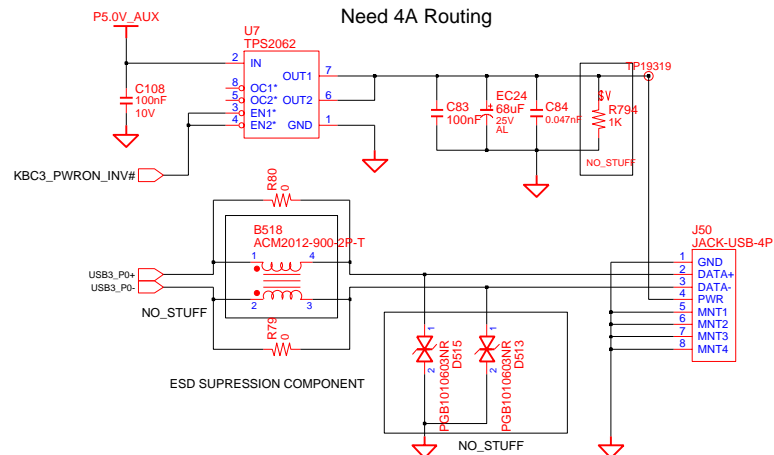
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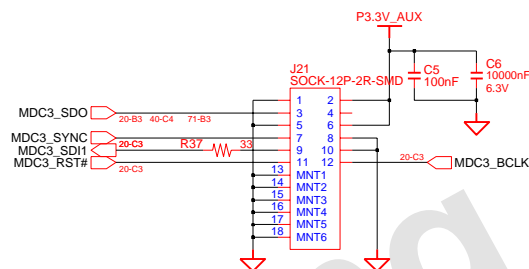
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2	CONNECTOR		
APPROVAL	KEVIN LEE	REV	1.0	HDD & ODD CONNECTOR	PART NO. BA41-XXXXX	
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM		PAGE 53 OF 58	

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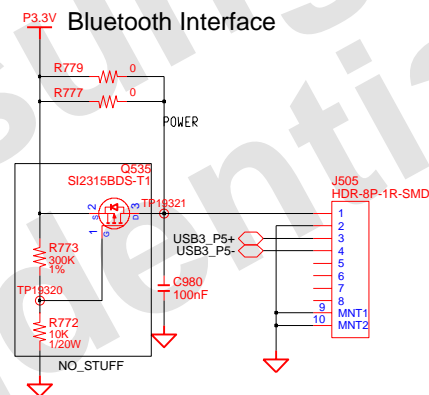
## 1 PORT USB CONNECTOR



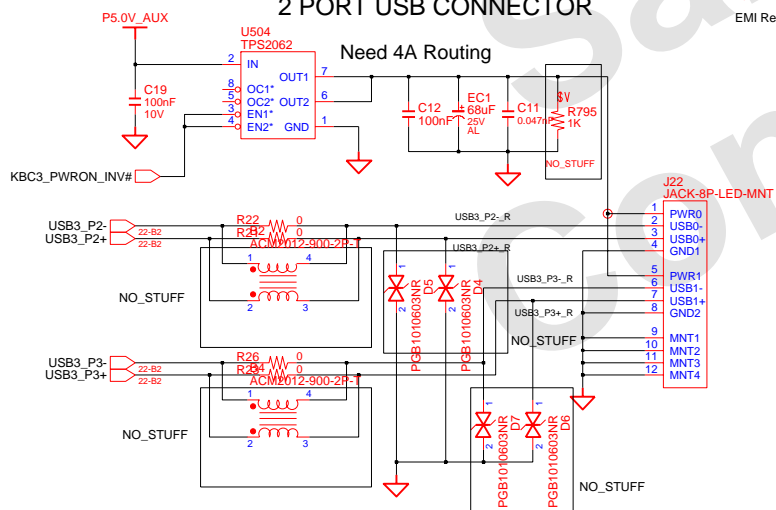
## MDC Connector



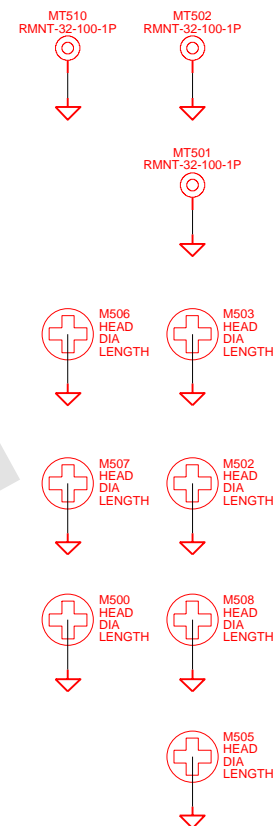
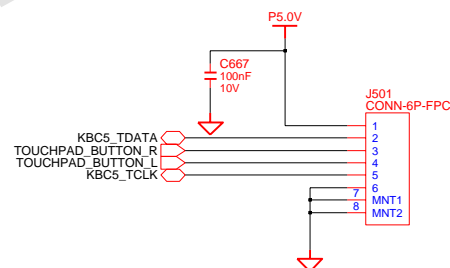
## Bluetooth Interface



## 2 PORT USB CONNECTOR

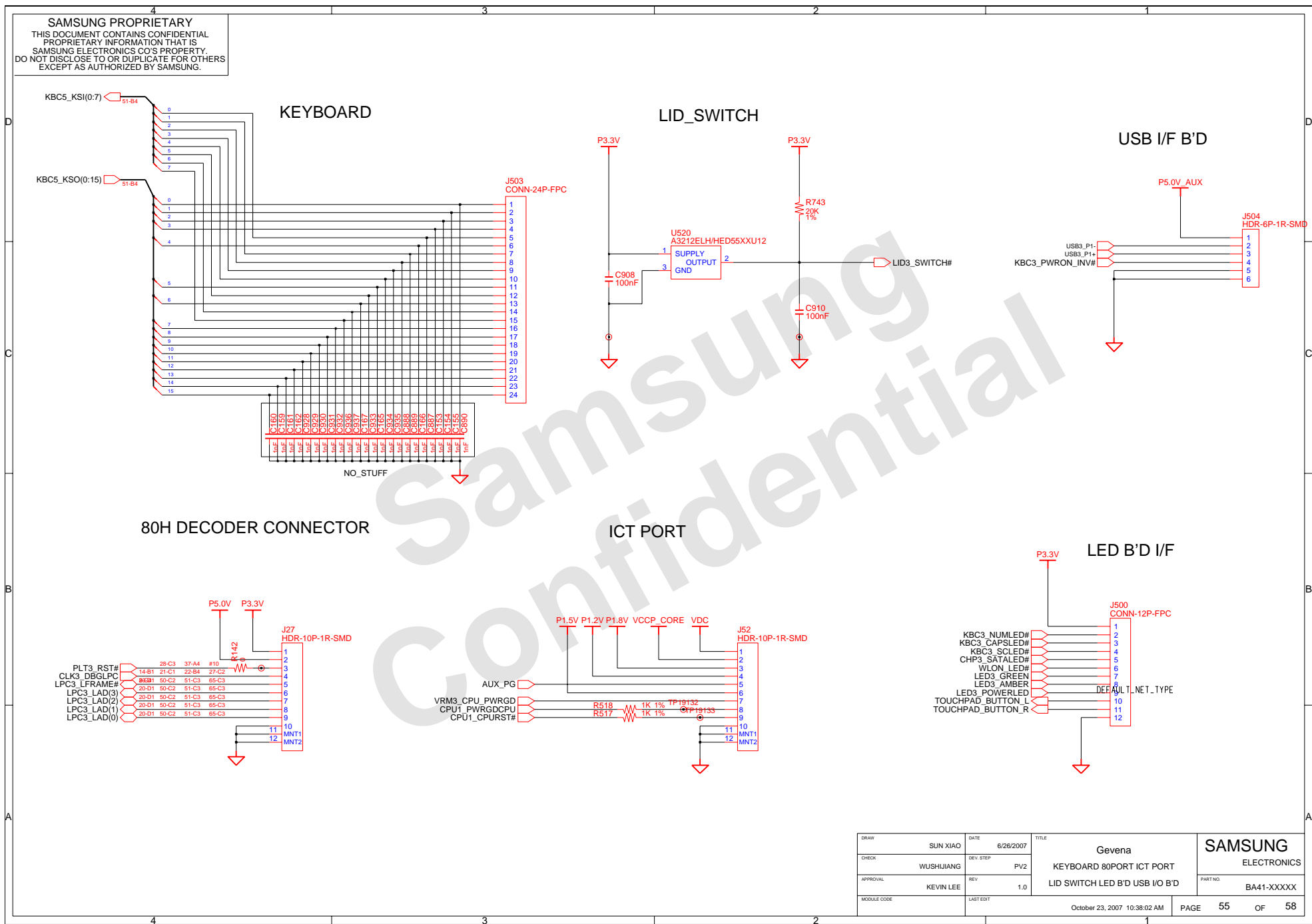


## TOUCHPAD CONNECTOR



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHUJIANG	DEV. STEP	PV2	USB MDC &	USB MDC &	ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0	TOUCHPAD BLUETOOTH I/F	PART NO.	BA41-XXXXX
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	54 OF 58

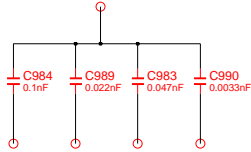
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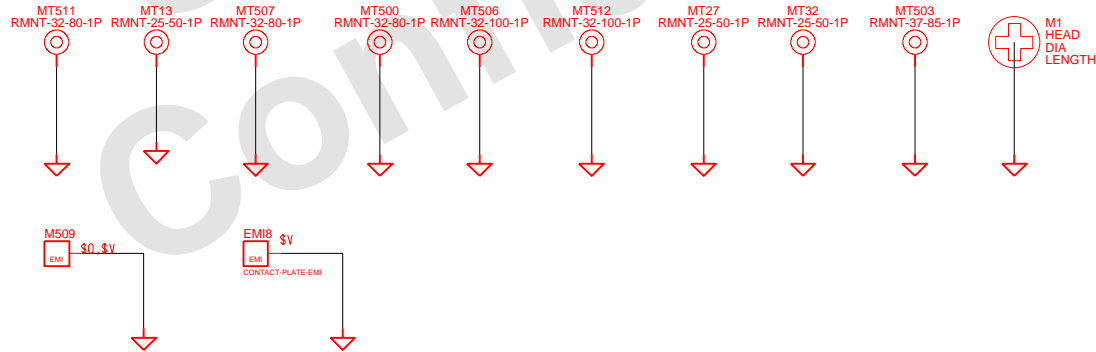
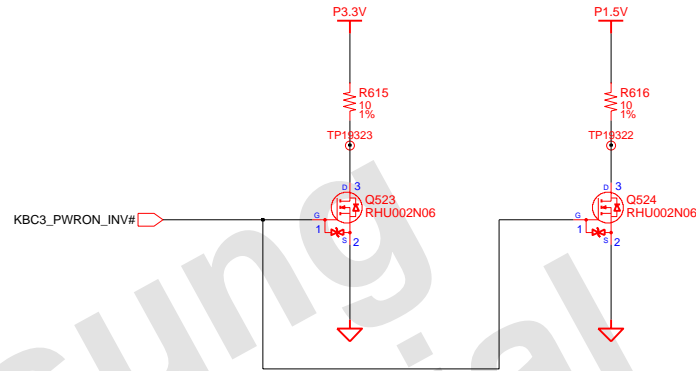
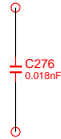
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHUJIANG	DEV. STEP	PV2	KEYBOARD 80PORT ICT PORT		ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0	LID SWITCH LED B'D USB I/O B'D	PART NO.	BA41-XXXXX
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	55	OF 58

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TOP SIDE



BOTTOM SIDE

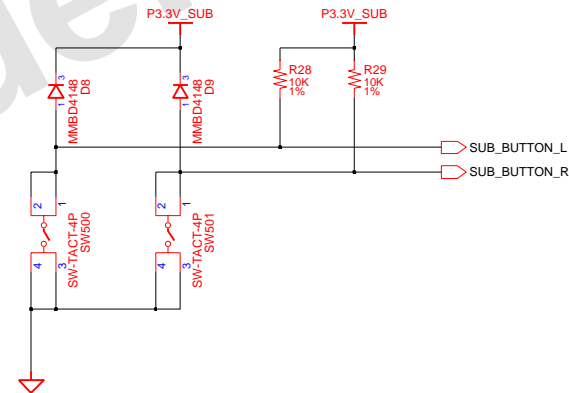
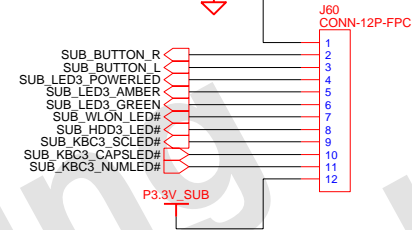
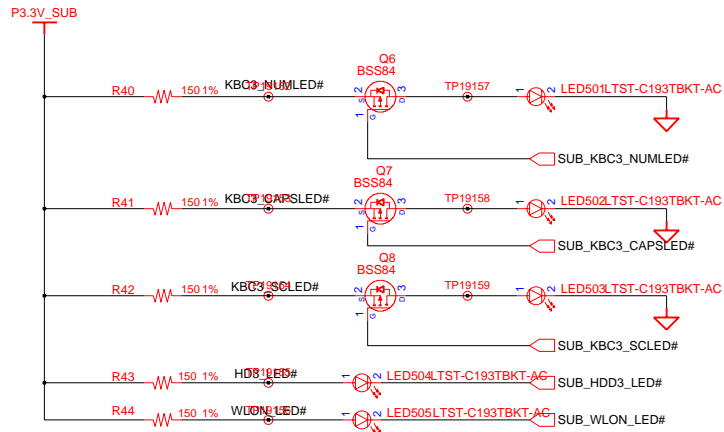


DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena OTHERS	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-XXXXX
CHECK	WUSHIJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	56 OF 58	



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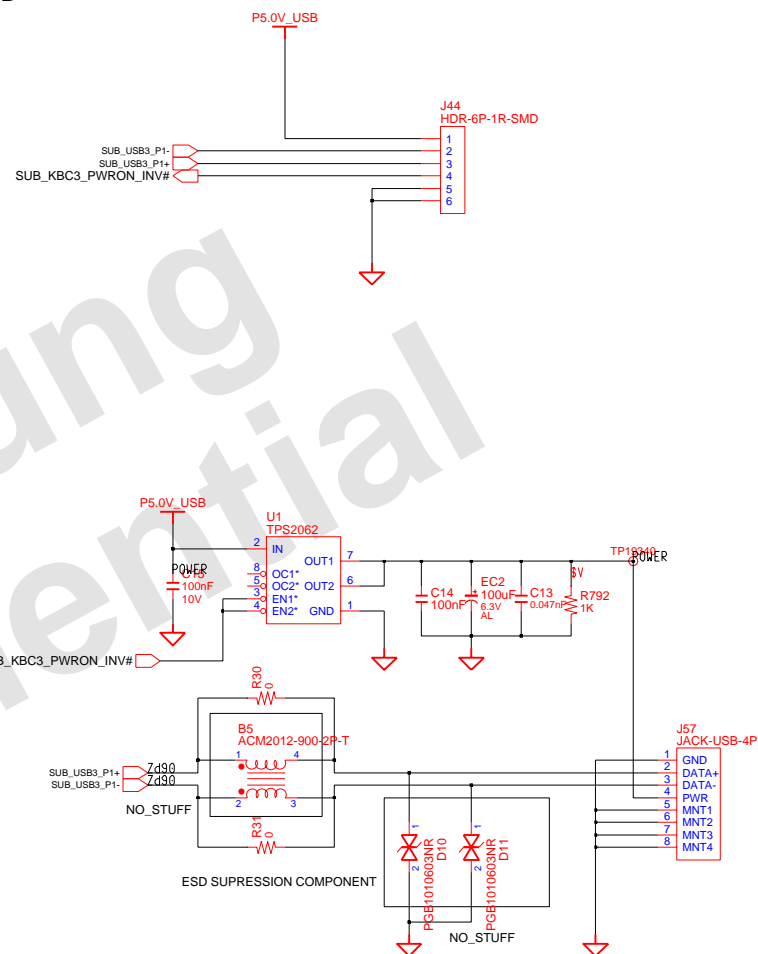
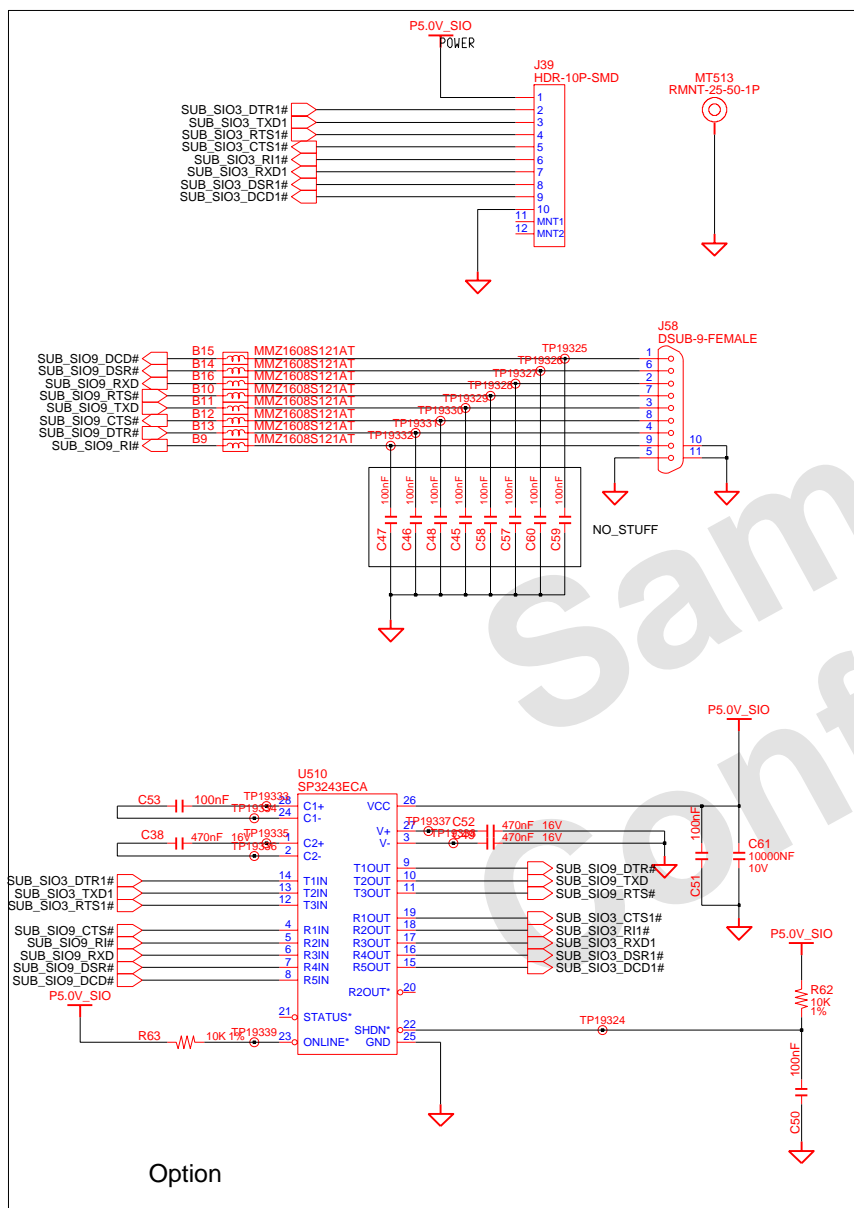
## TOUCHPAD AND LED B'D



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-
CHECK	WUSHIJIANG	DEV. STEP	PV2	TOUCHPAD AND LED B'D		
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE	LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	57 OF 60	

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## SIO AND USB SUB B'D



DRAW	SUN XIAO	DATE	6/30/2007	TITLE Geneva MIO BOARD USB AND SIO SUB B'D	<b>SAMSUNG</b> ELECTRONICS
CHECK	WUSHIJIANG	DEV. STEP	PV2		
APPROVAL	KEVIN LEE	REV	1.0		
MODULE CODE	LAST EDIT		October 23, 2007 10:38:02 AM		
				PART NO.	BA41-undefined

TP18380OAU3\_SEL  
TP18381OAU3\_BCLK  
TP18382OAU3\_BEEP  
TP18383OAU3\_BEEP\_CU  
TP18384OAU3\_GP100#  
TP18385OAU3\_GP101#  
TP18386OAU3\_GP101#\_L  
TP18387OAU3\_RST#  
TP18388OAU3\_SDIO  
TP18389OAU3\_SDIO\_RU  
TP18390OAU3\_SDO  
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DRAW	SUNXIAO	DATE	9/10/2007	TITLE	Gevena TEST POINT	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41 - undef ined
CHECK	WUSHIJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	59 OF 59	

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 EXCEPT AS AUTHORIZED BY SAMSUNG.

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TP18541 ○ MODEM\_TIP\_BCON

[illegible]

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T1961845 P1.8V_AUX_RCOMP#_R
T1961846 P1.8V_AUX_RCOMP_E_R
T1961847 P1.8V_AUX_RCOMP_VOH_R
T1961848 P1.8V_AUX_RCOMP_VOL_R
T1961849 P1.8V_AUX_VCC_SM_CK
T1962020 P5.0V_ALW_SREF_SUS
T1962021 P5.0V_ALW_SREF_SUS
T1962022 P5.0V_AU_GHC
T1962023 P5.0V_AU_GHC
T1962024 P5.0V_AU_GHC
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 TP181333 SC452 BS15  
 TP181434 SC452 FB2  
 TP181535 SC452 ISH  
 TP181636 SC452 SS  
 TP181737 SC452 V1  
 TP181838 SC452 VP2N2  
 TP181939 SC452 VREF  
 TP182040 SC103 CDS1  
 TP182141 SC103 CDS11  
 TP182242 SC103 CDS12  
 TP182343 SC103 DIR1  
 TP182444 SC103 RT1  
 TP182545 SC103 RT1  
 TP182646 SC103 RT1  
 TP182747 SC103 TXD1  
 TP182848 SMP3 ALERT#  
 TP182949 SMP3 CLK  
 TP183050 SMP3 DA  
 TP183151 SMP3 D1  
 TP183252 SMP3 ME-DLA

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TP19054VRVR33_CPU_PWRGD
TP19055VTVT13_PWRGD
TP18230MLMLON_LED#
TP18232IOIO_7VDD0A
TP18235OCOC_REF
TP18241CND2CND2
TP18242CND2CND2
TP18245OCOC_AUD
TP18198OCOC_CPU
TP18200OCOC_CPU
TP18204OCOC_DDR
TP18206OCOC_P1_25V
TP18212OCOC_P1_5V
TP18217OCOC_P3_3V
TP18222LCDLCD_VDD03V
TP18223LCDLCD_VDD03V
TP18224OCOC_P2_5V
TP18225OCOC_P2_5V
TP18116PRTCPRTC_BAT
TP18122OVOV_PSS_PL1_VDD
TP18124OVCCOVCC_CORE
TP18125OVCCOVCC_CORE
TP18130OVCCOVCC_CRT
TP18131OVCCOVCC_CRT
TP18081OVDCOVDC
TP18084OVDCADPT
TP18085OVDCINV
TP18086OVDCINV
TP18098OVDDOVDD_AUD

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TP18164OP0.9V  
TP18170OP1.05V\_PEG  
TP18172OP1.25V  
TP18178OP1.2V  
TP18183OP1.5V  
TP18187OP1.5V\_EXP  
TP18188OP1.8V  
TP18192OP1.8V\_ALW  
TP18134OP12.0V\_ALW  
TP18136OP3.3V\_ALW  
TP18141OP3.3V\_AUX\_EXP  
TP18146OP3.3V\_EXP  
TP18150OP3.3V\_MCD  
TP18152OP3.3V\_MICOM  
TP18158OP3.3V\_USB  
TP18161OP5.0V\_ALW  
TP18104OP5.0V\_ALW  
TP18109OP5.0V\_SIO  
TP18112OP5.0V\_USB

DATE	9/10/2007	TITLE	Gevena TEST POINT			
CHECK	WUSHUIJIANG, PV2	DEV. STEP			PART NO. BA41-undef i	
APPROVAL	KEVIN.LEE, 1.0	REV				
MODULE CODE	LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	60	OF 60

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